FIG.1

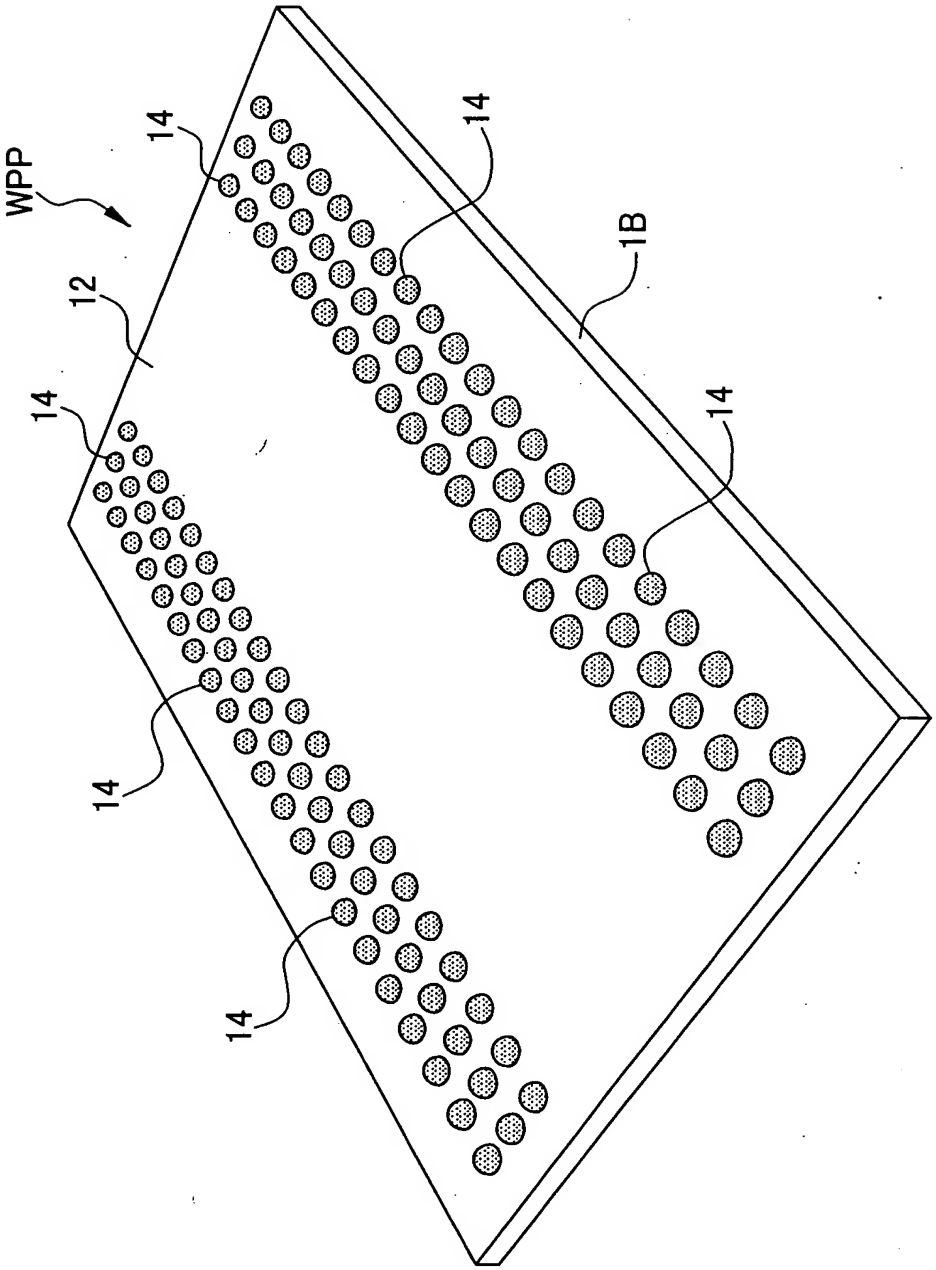


FIG.2

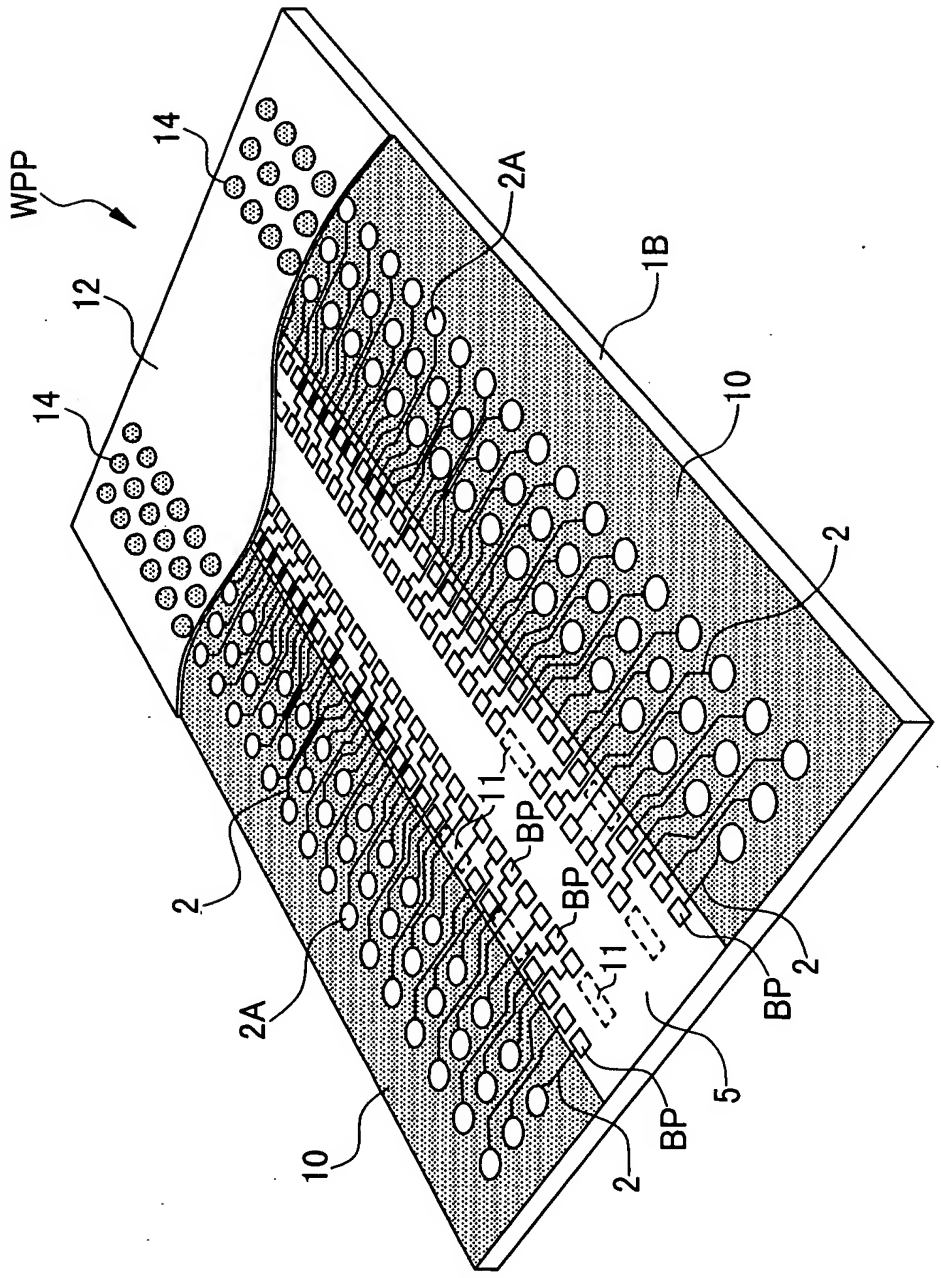


FIG.3

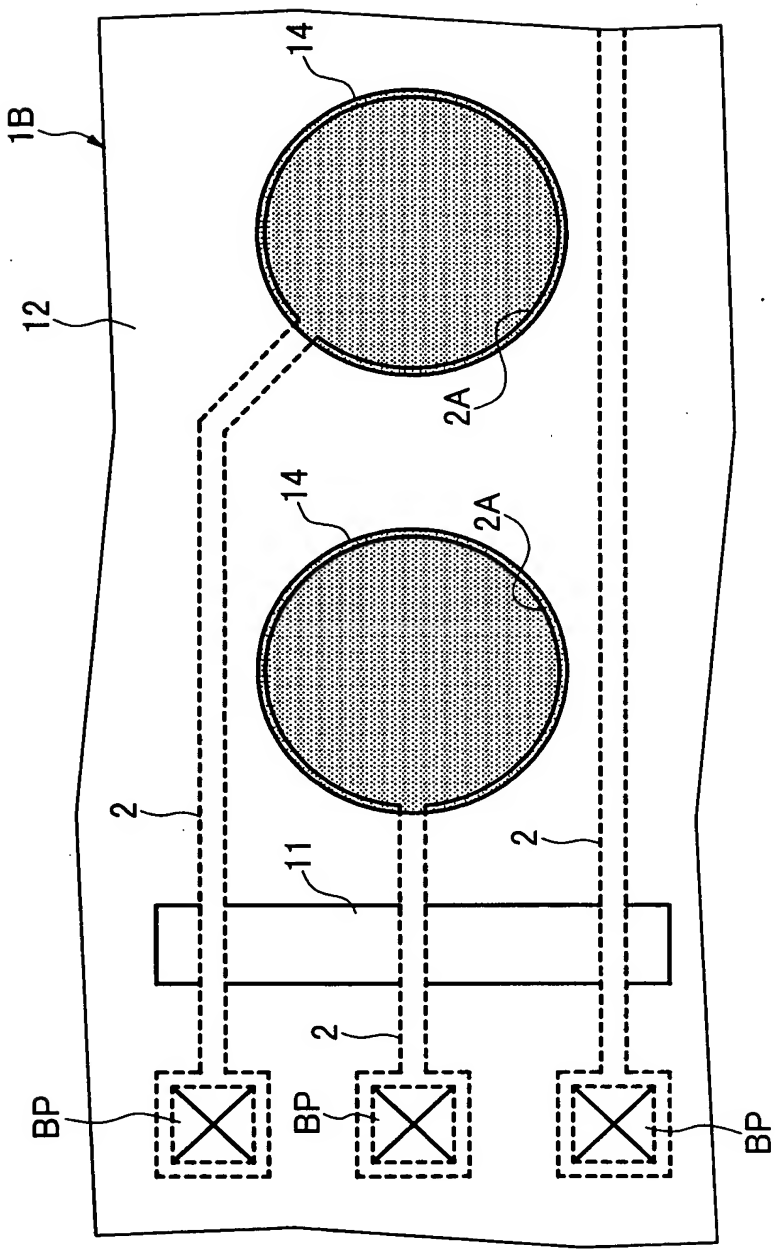


FIG.4

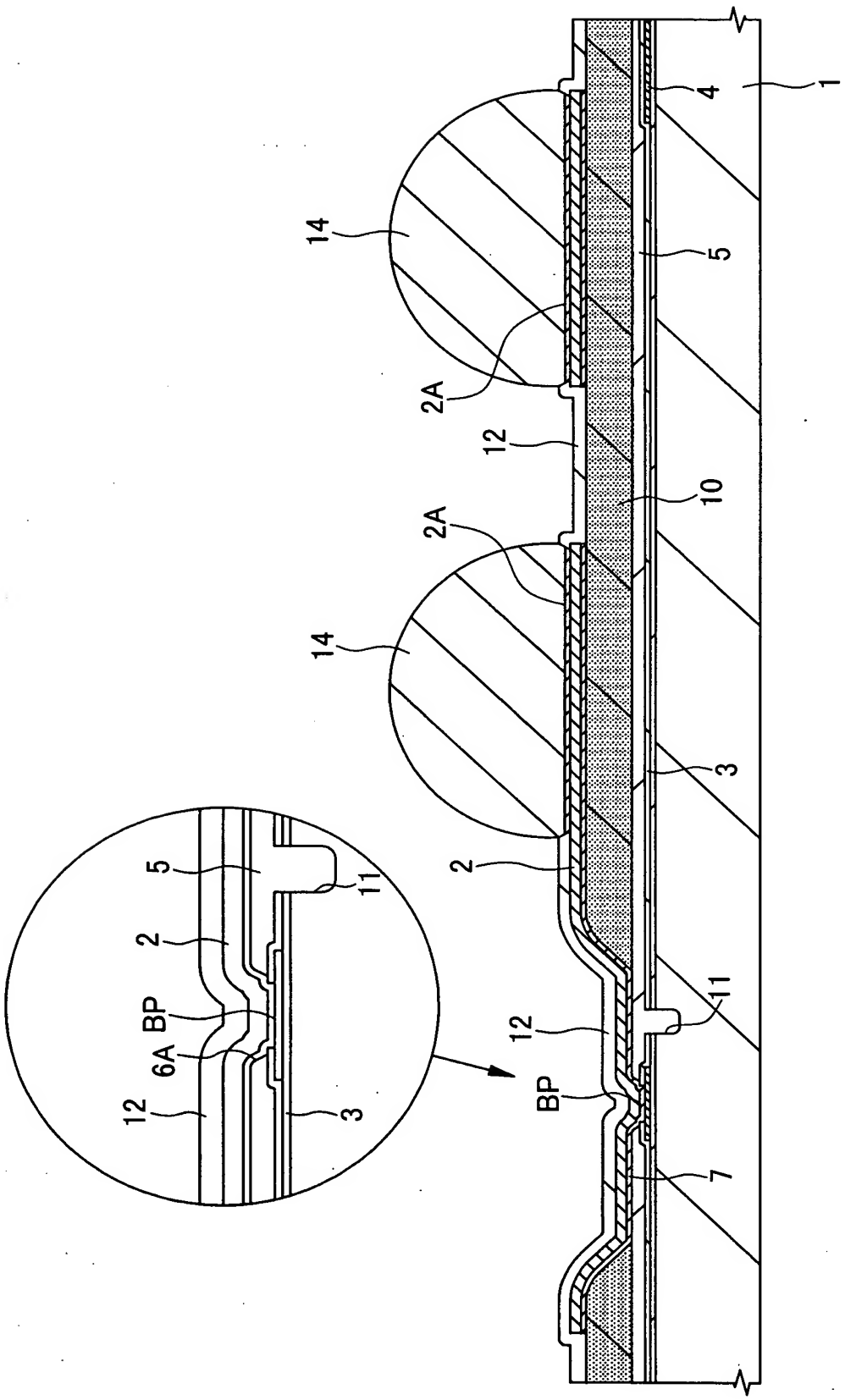


FIG.5

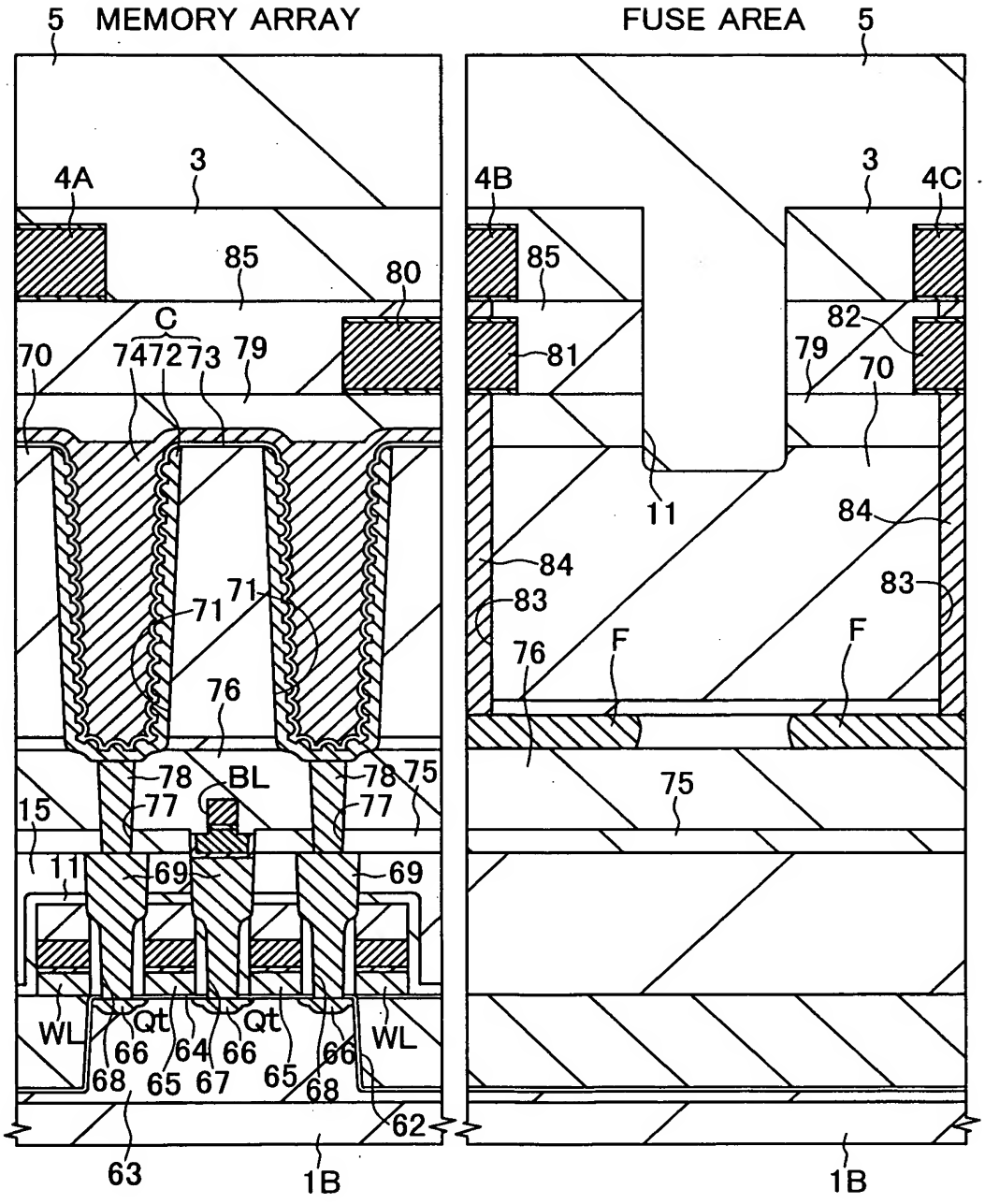

5 MEMORY ARRAY
FUSE AREA 5
4A
3
4B
3
4C
85
80
85
82
C
74
72
73
79
81
79
70
70
11
84
84
83
83
71
71
76
F
F
76
78
BL
78
75
75
77
77
15
11
69
69
WL
Qt
Qt
WL
66
64
66
66
68
65
67
65
68
62
63
1B
1B

FIG.6

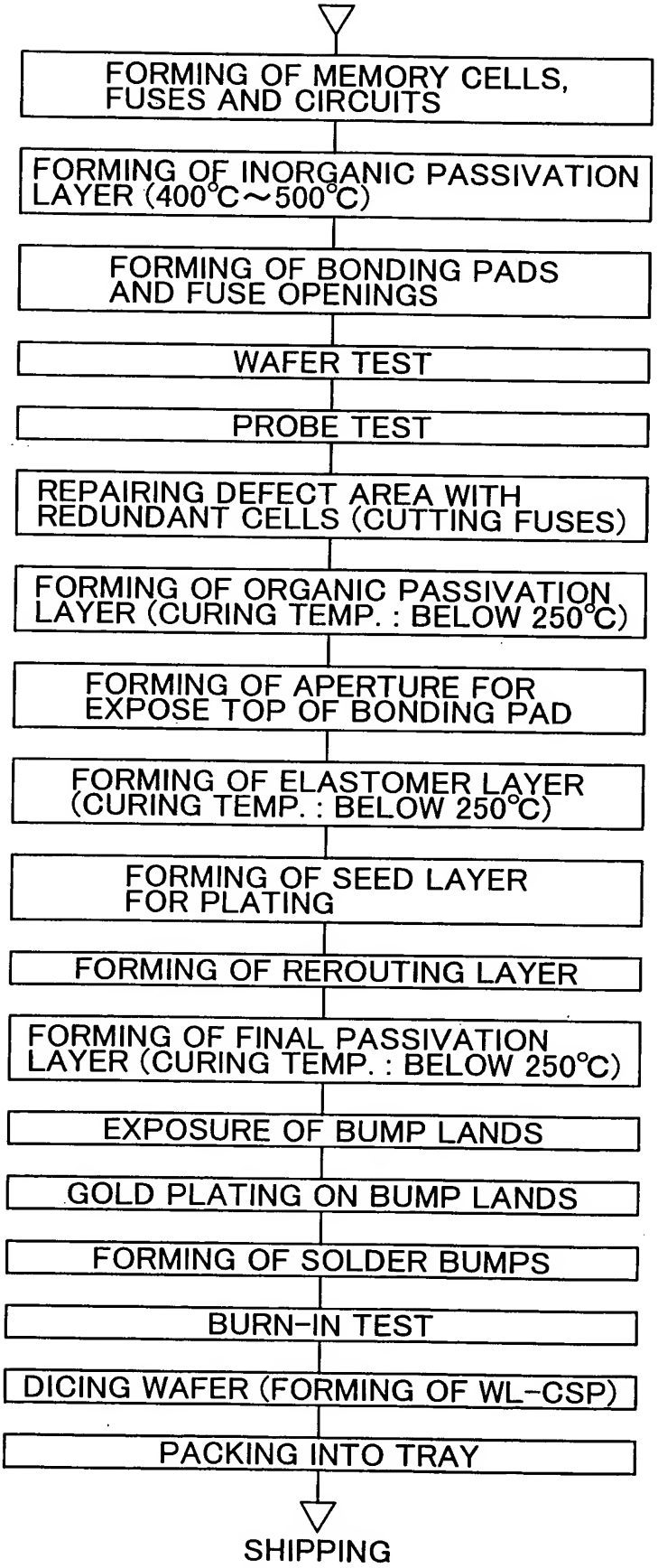

FORMING OF MEMORY CELLS, FUSES AND CIRCUITS
FORMING OF INORGANIC PASSIVATION LAYER (400°C~500°C)
FORMING OF BONDING PADS AND FUSE OPENINGS
WAFER TEST
PROBE TEST
REPAIRING DEFECT AREA WITH REDUNDANT CELLS (CUTTING FUSES)
FORMING OF ORGANIC PASSIVATION LAYER (CURING TEMP. : BELOW 250°C)
FORMING OF APERTURE FOR EXPOSE TOP OF BONDING PAD
FORMING OF ELASTOMER LAYER (CURING TEMP. : BELOW 250°C)
FORMING OF SEED LAYER FOR PLATING
FORMING OF REROUTING LAYER
FORMING OF FINAL PASSIVATION LAYER (CURING TEMP. : BELOW 250°C)
EXPOSURE OF BUMP LANDS
GOLD PLATING ON BUMP LANDS
FORMING OF SOLDER BUMPS
BURN-IN TEST
DICING WAFER (FORMING OF WL-CSP)
PACKING INTO TRAY
SHIPPING

FIG.7

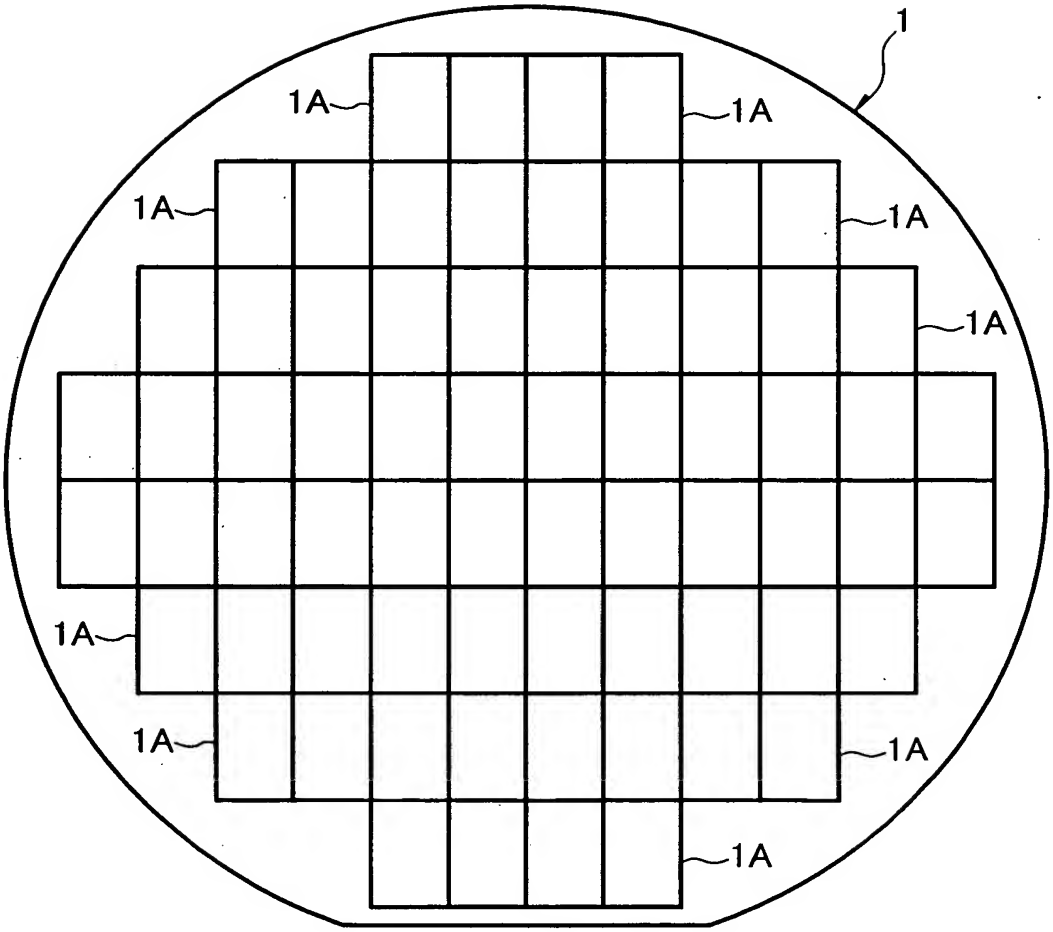


FIG.8

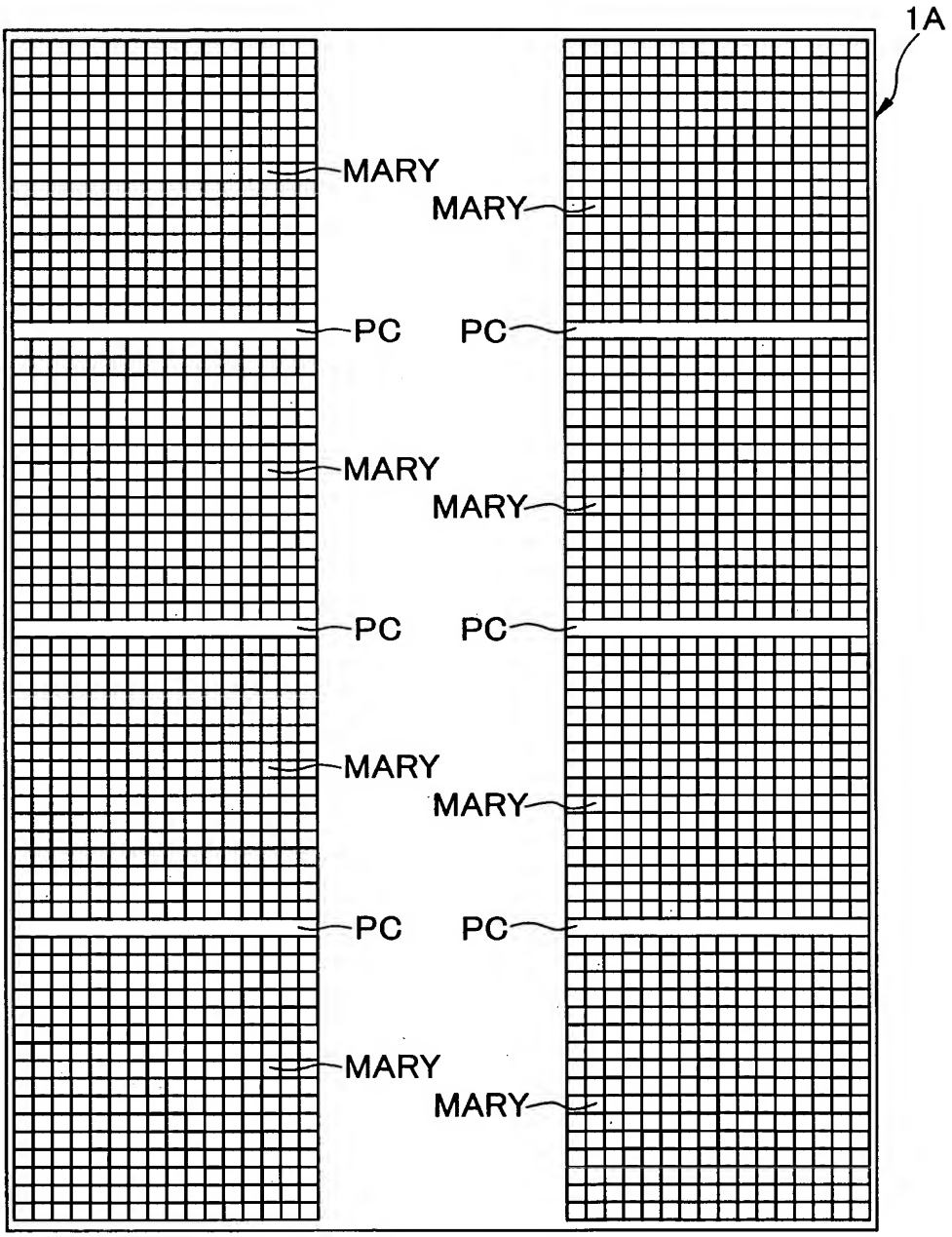


FIG.9

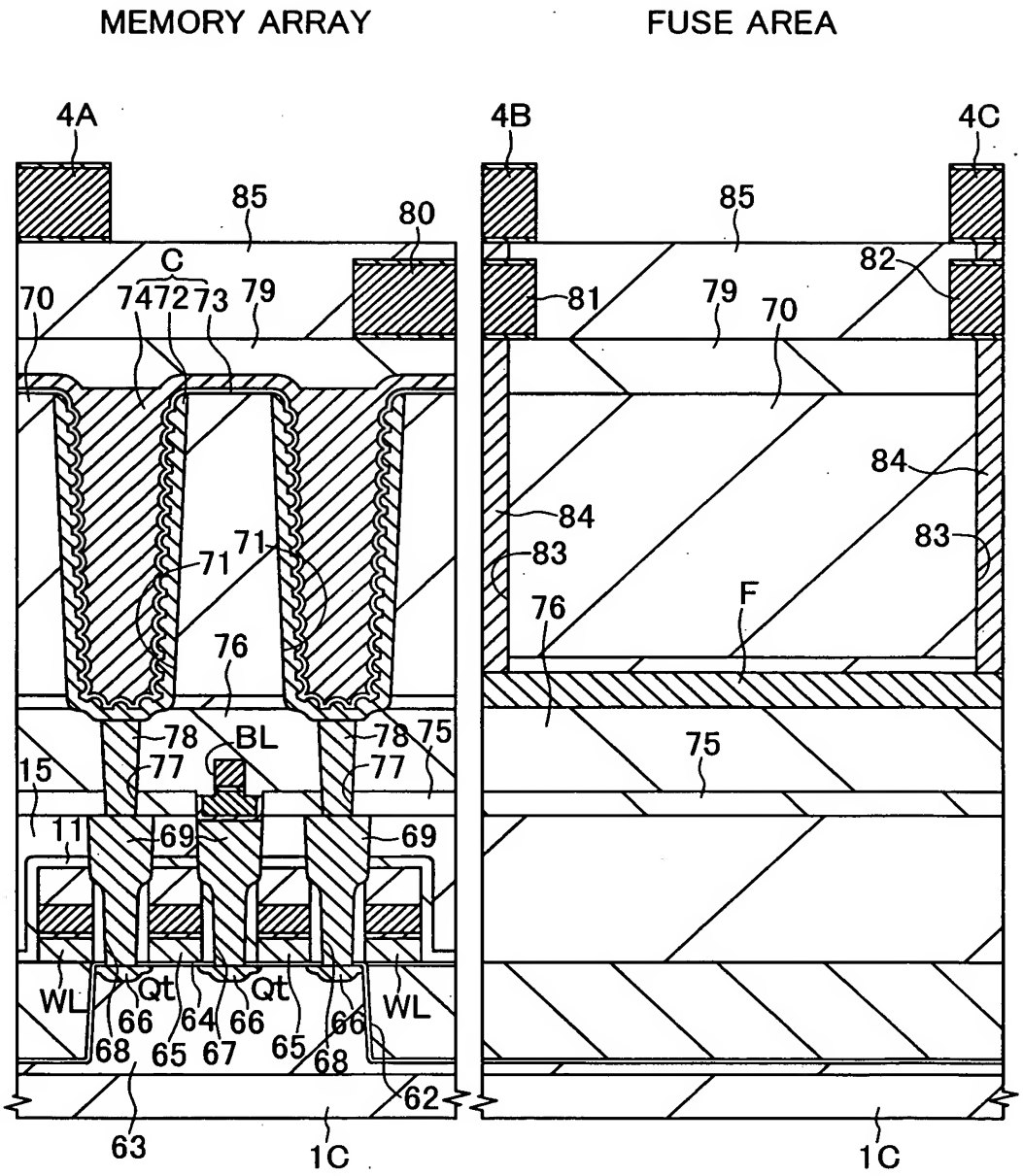

MEMORY ARRAY
FUSE AREA
4A
4B
4C
85
80
C
70
74
72
73
79
81
82
71
76
78
BL
77
75
15
11
69
WL
Qt
66
64
67
65
68
62
63
1C
84
83
F

FIG.10

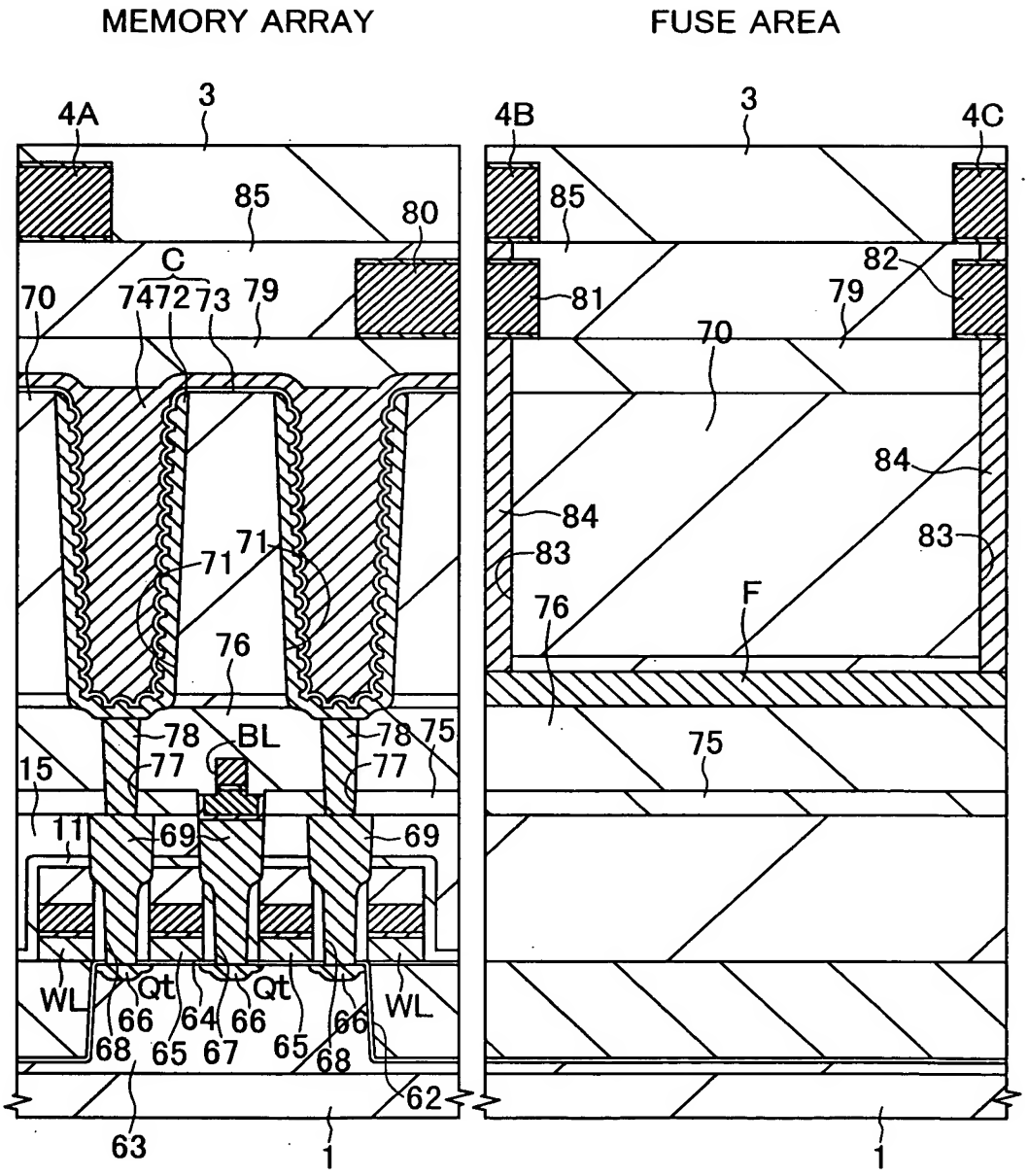

MEMORY ARRAY
FUSE AREA
4A
3
4B
3
4C
85
80
85
82
C
70
74
72
73
79
81
79
70
84
84
83
83
71
71
F
76
76
78
BL
78
75
77
77
75
15
11
69
69
WL
Qt
Qt
WL
66
64
66
66
68
65
67
65
68
62
63
1
1

FIG.11

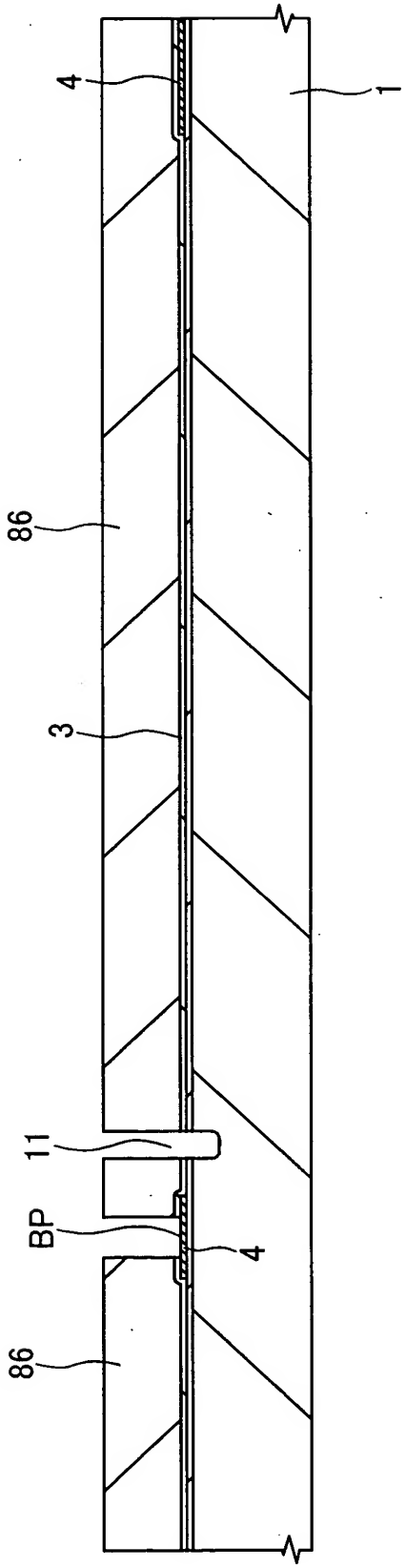
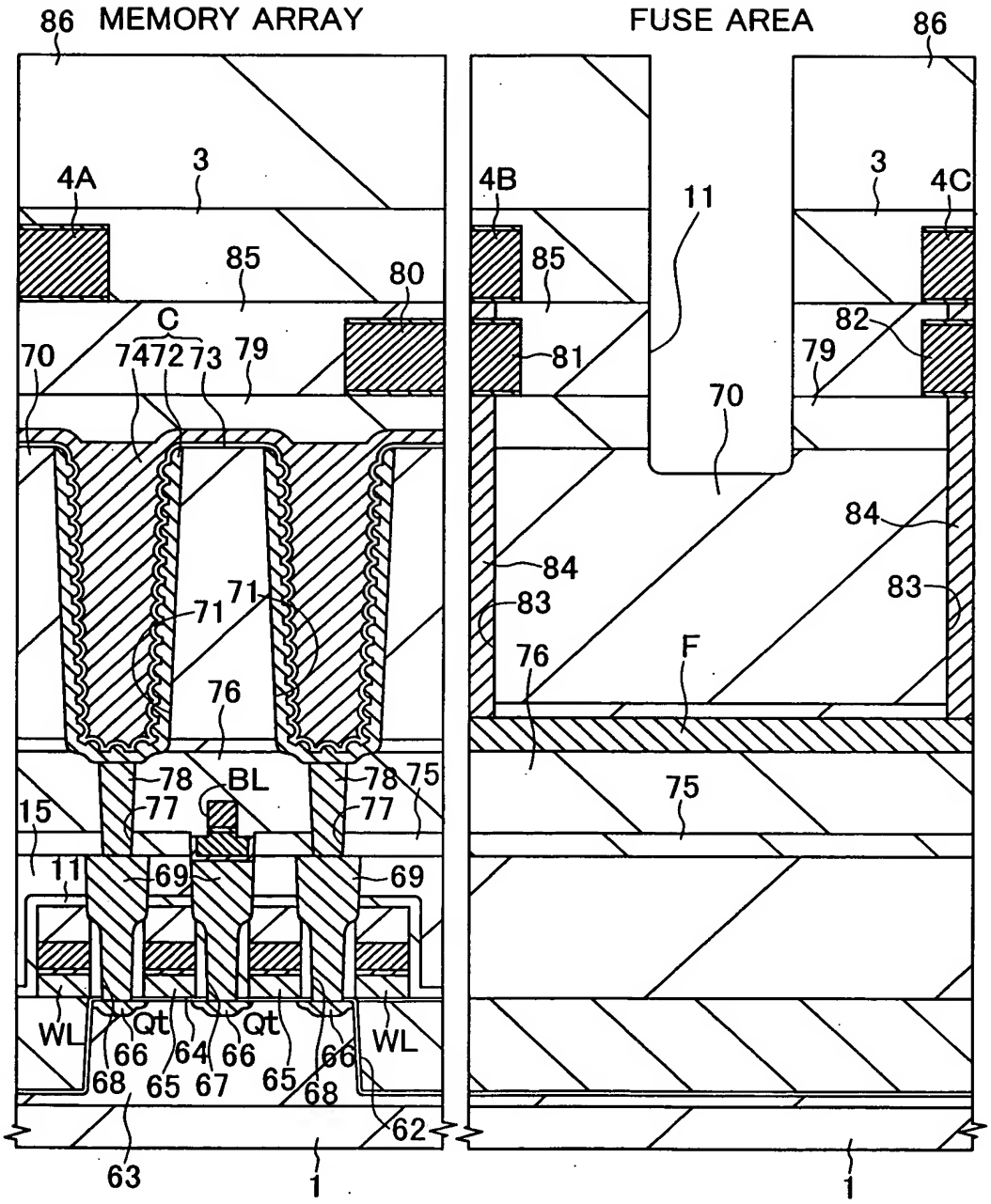


FIG.12


86
MEMORY ARRAY
FUSE AREA
86
4A
3
4B
11
3
4C
85
80
85
82
C
70
74
72
73
79
81
79
70
84
84
71
71
83
83
76
F
76
78
BL
78
75
75
77
77
15
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69
69
WL
Qt
Qt
WL
66
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66
66
68
65
67
65
68
62
63
1
1

FIG.13

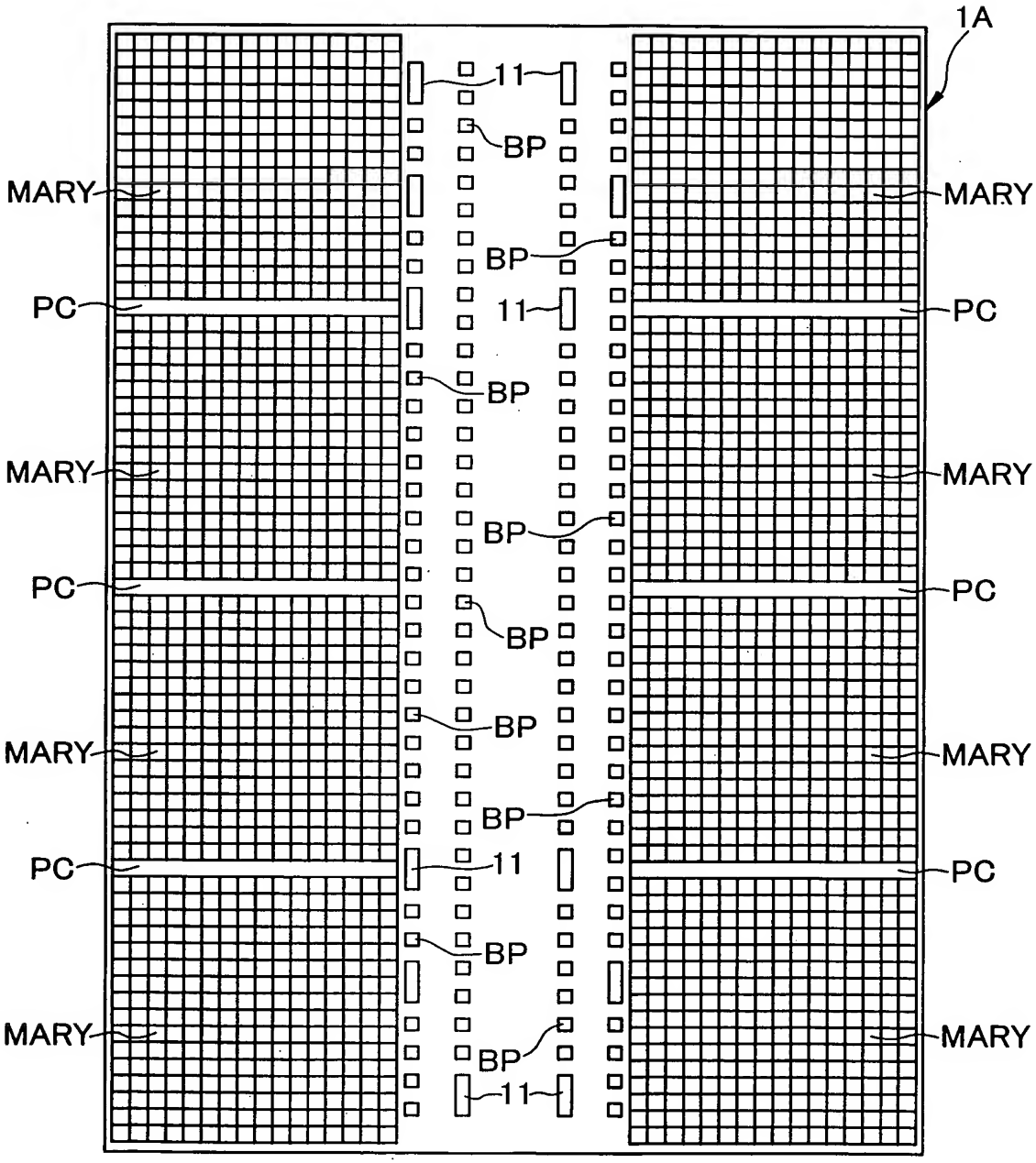
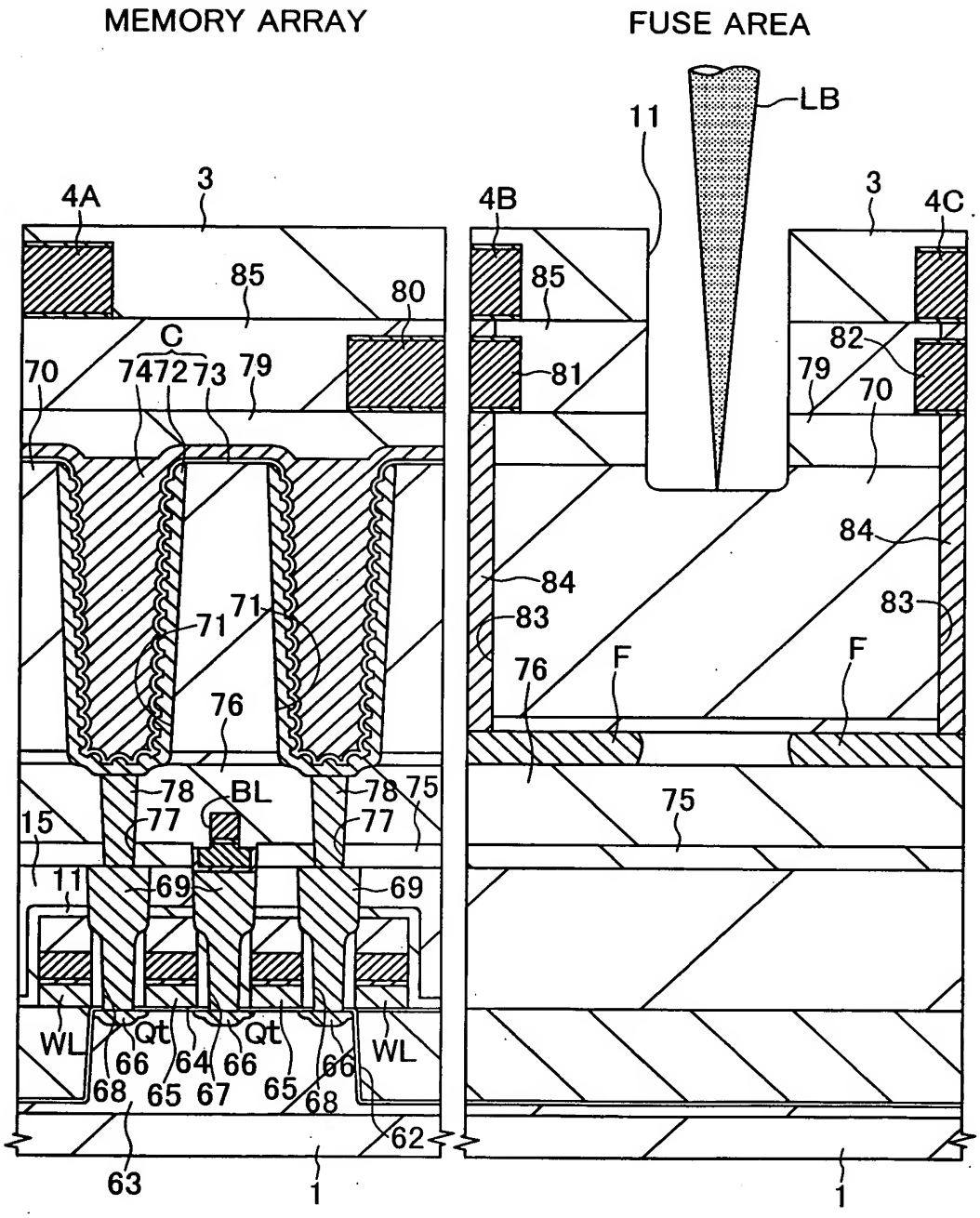


FIG.14


MEMORY ARRAY
FUSE AREA
LB
11
4A
3
4B
3
4C
85
80
85
C
82
70
74
72
73
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81
79
70
84
84
71
71
83
83
76
F
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76
78
BL
78
75
75
15
77
77
11
69
69
WL
Qt
Qt
WL
66
64
66
66
68
65
67
65
68
62
63
1
1

FIG.15

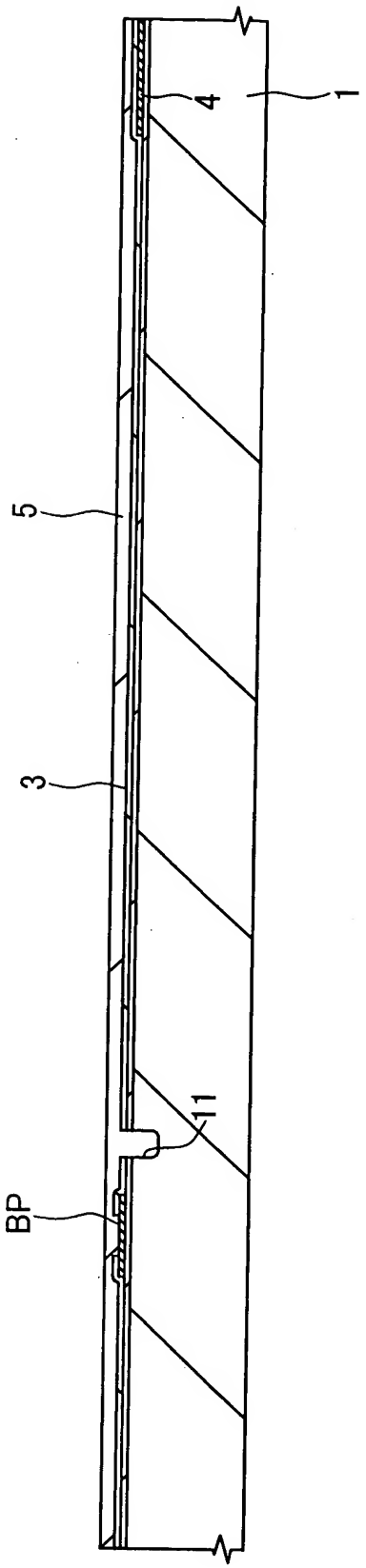
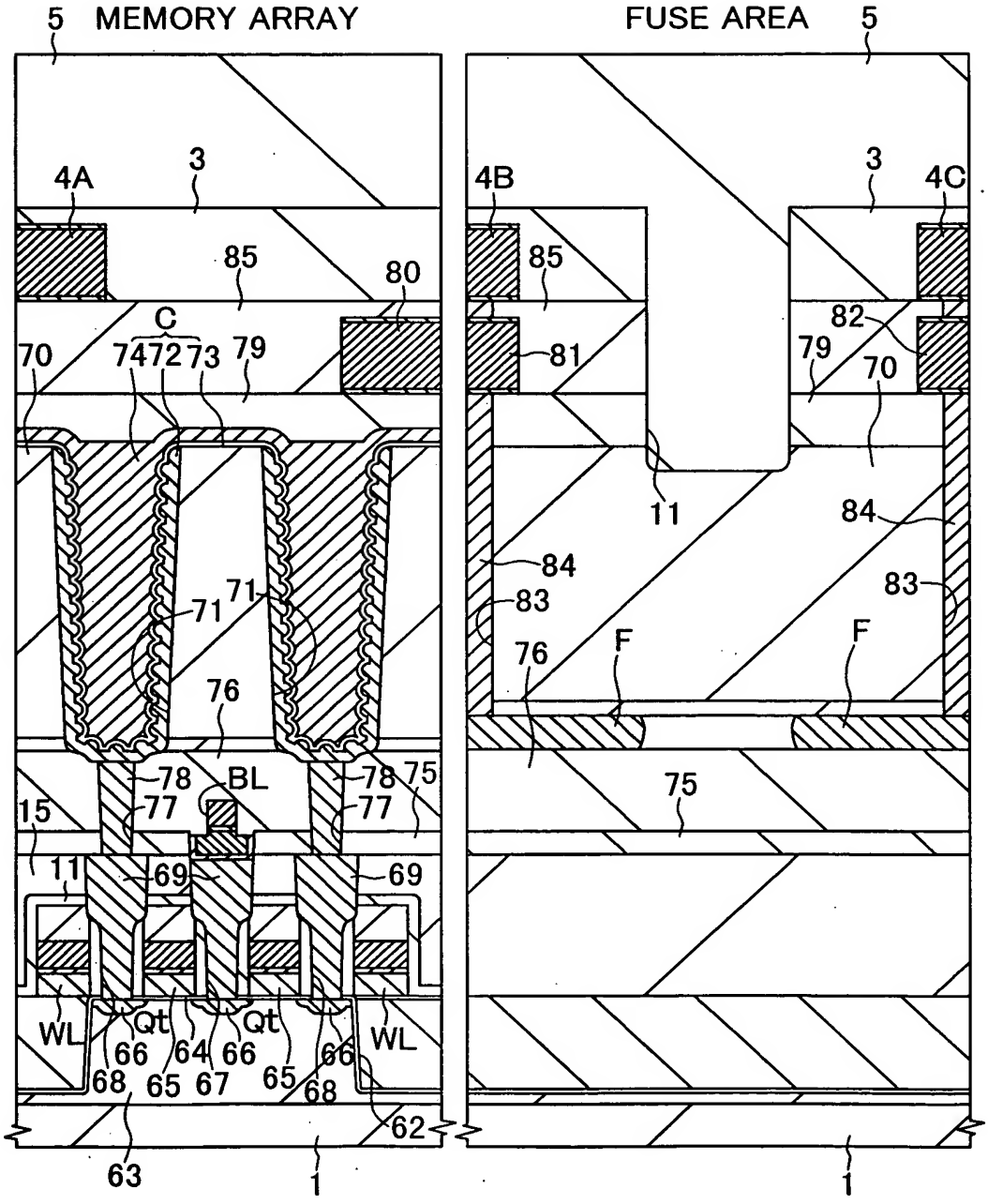


FIG.16


5 MEMORY ARRAY
FUSE AREA 5
4A
3
4B
3
4C
85
80
85
82
C
70
74 72 73
79
81
79
70
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84
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83
83
71
71
76
F
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76
78
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77
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WL
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Qt
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67
65
68
62
63
1
1

FIG.17

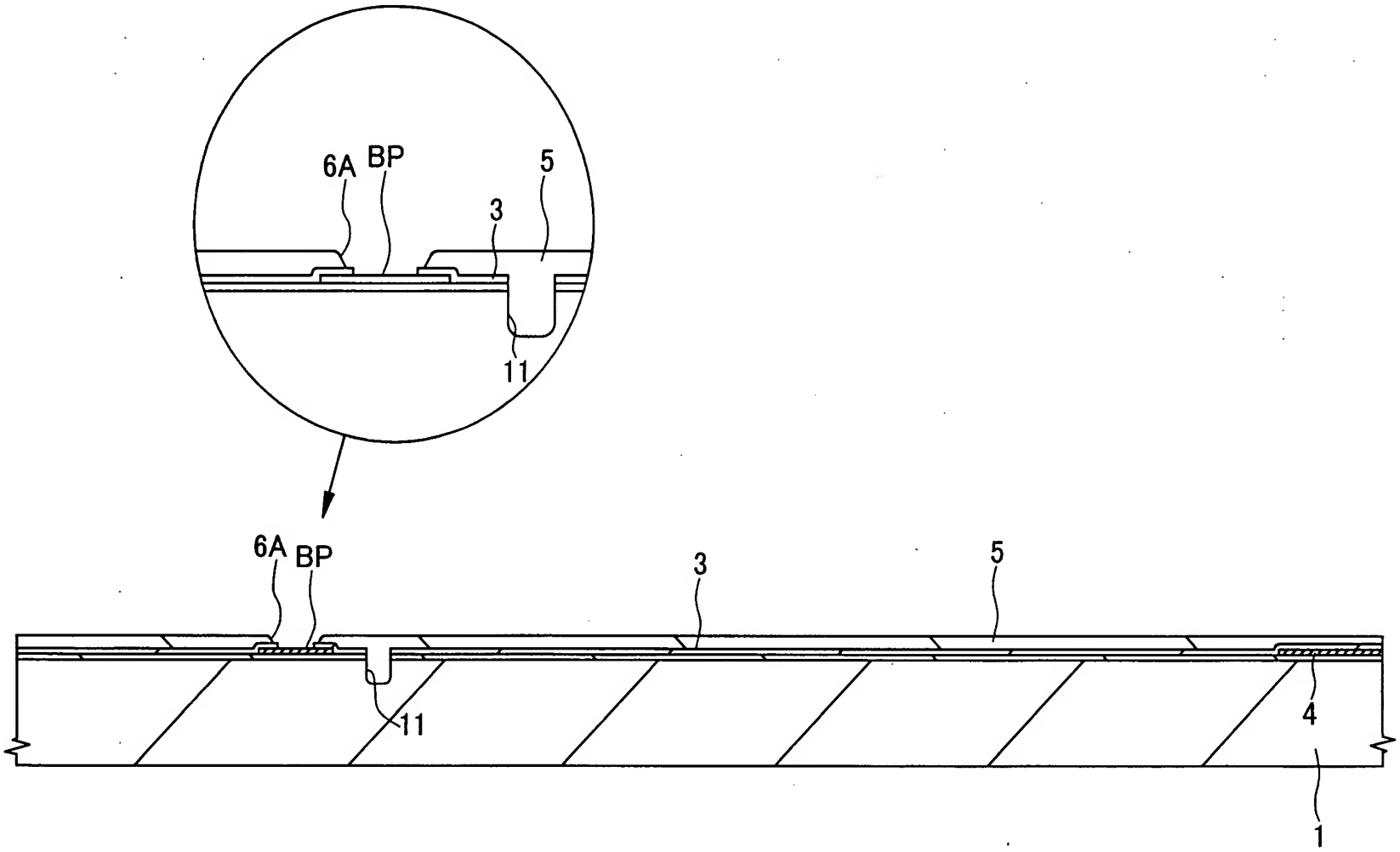


FIG.18

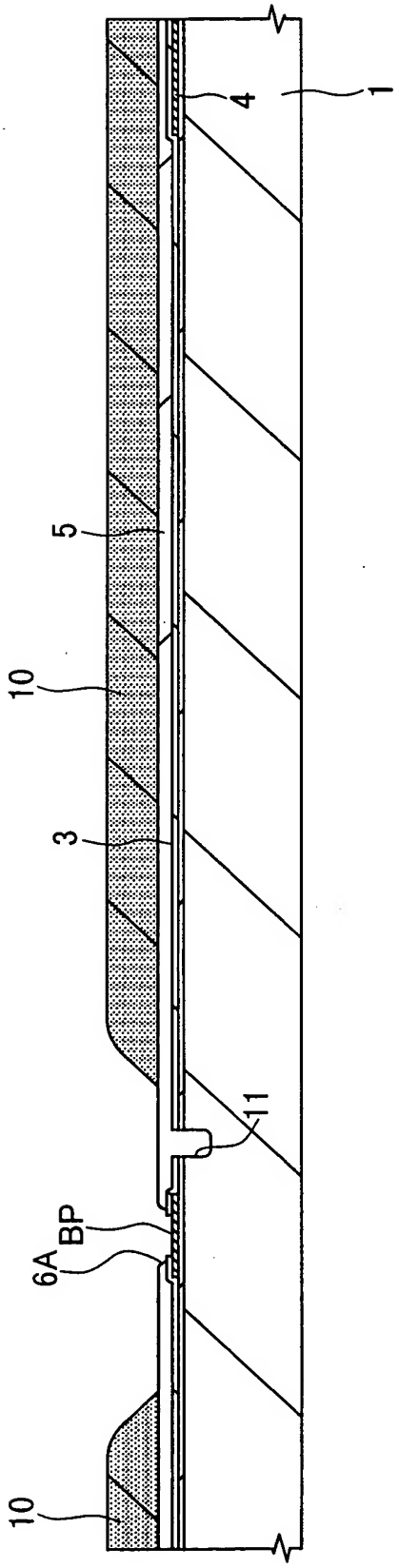


FIG.19

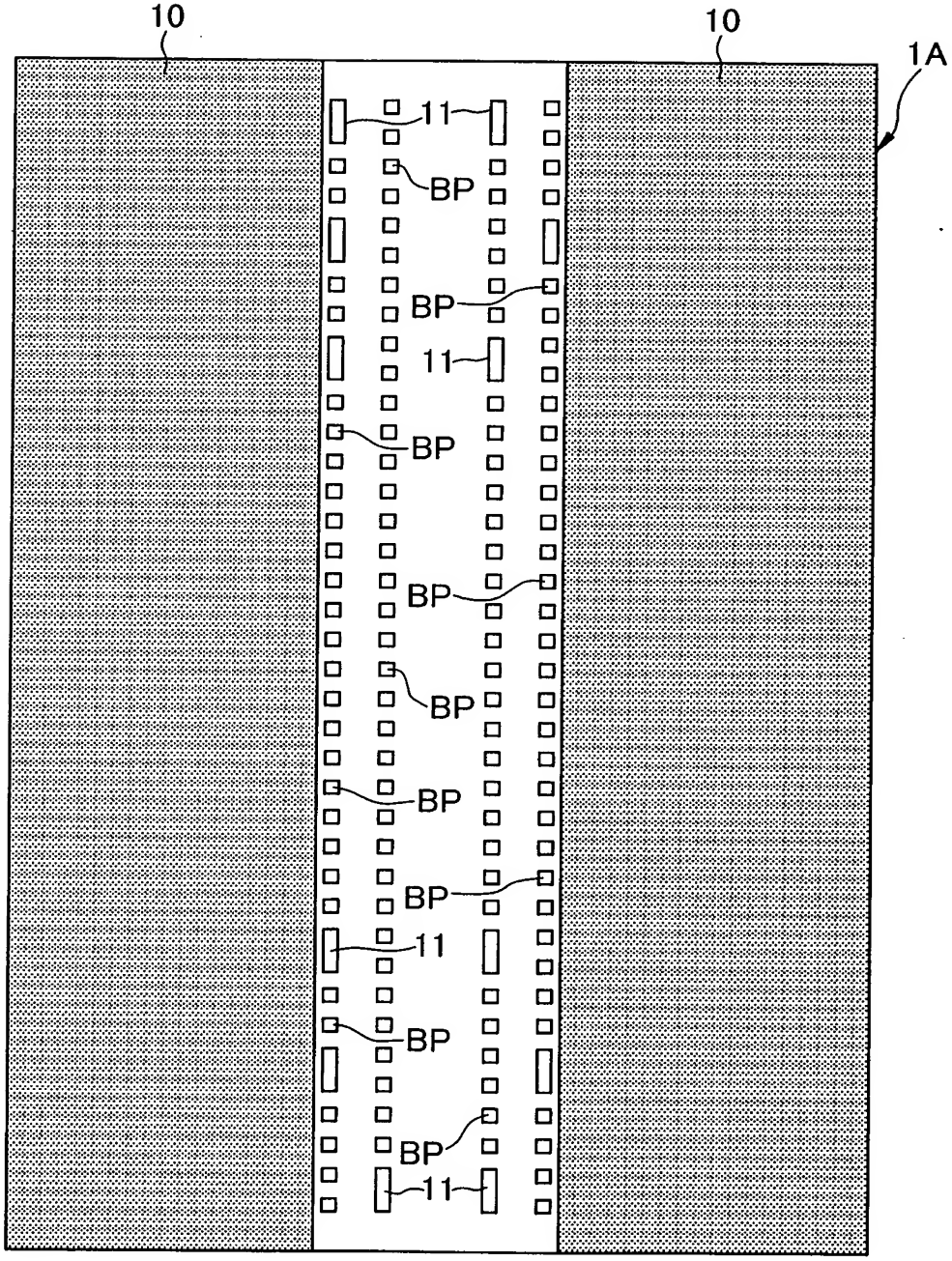


FIG.20

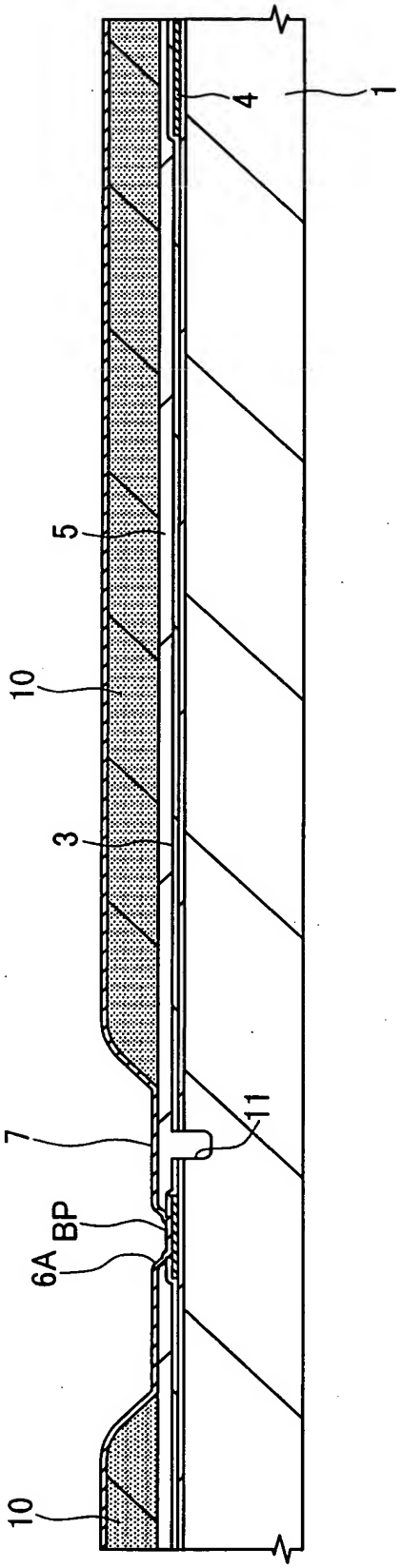


FIG.21

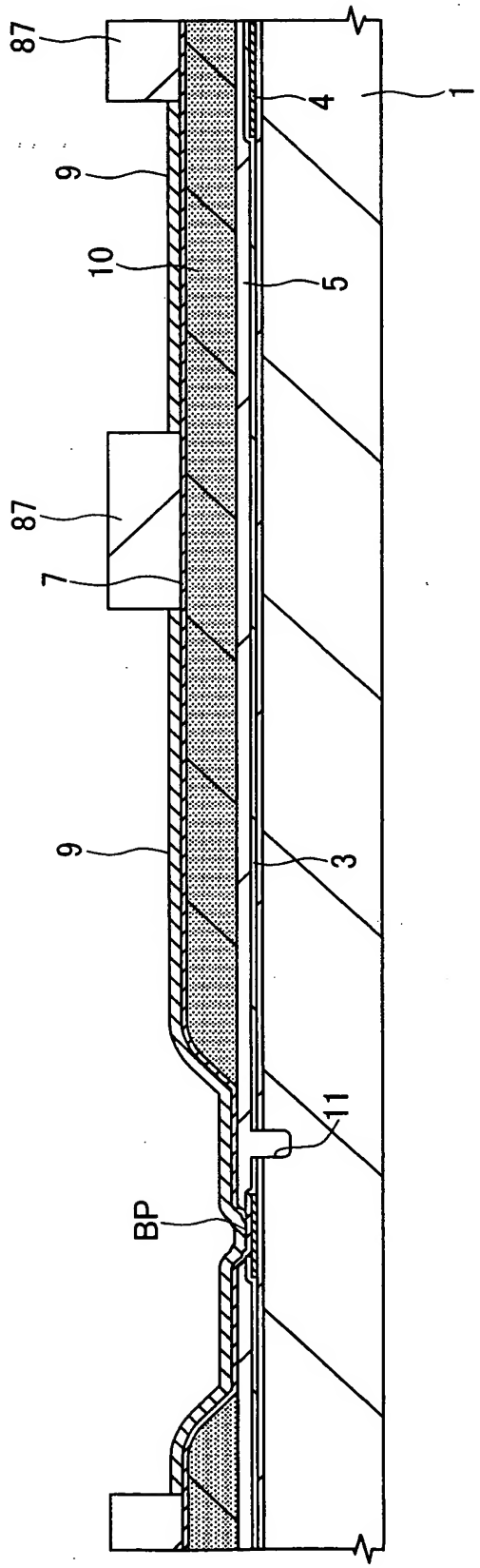


FIG.22

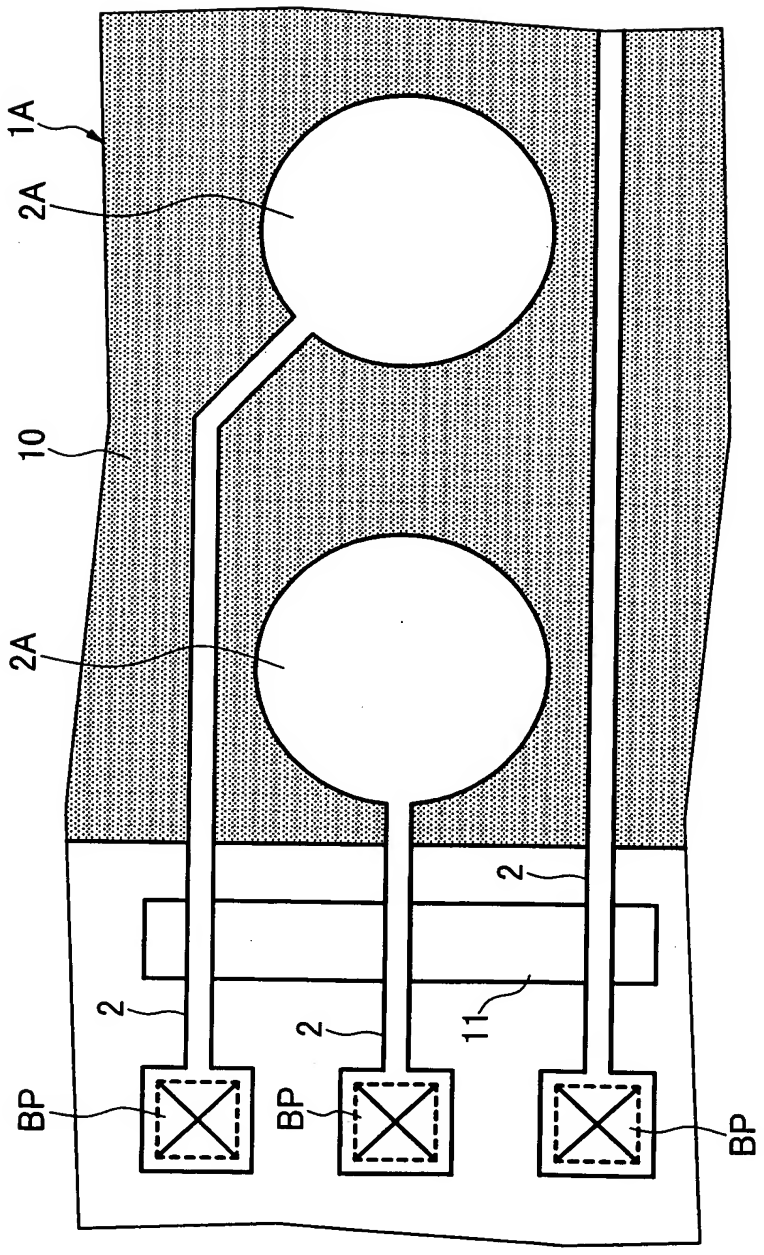


FIG.23

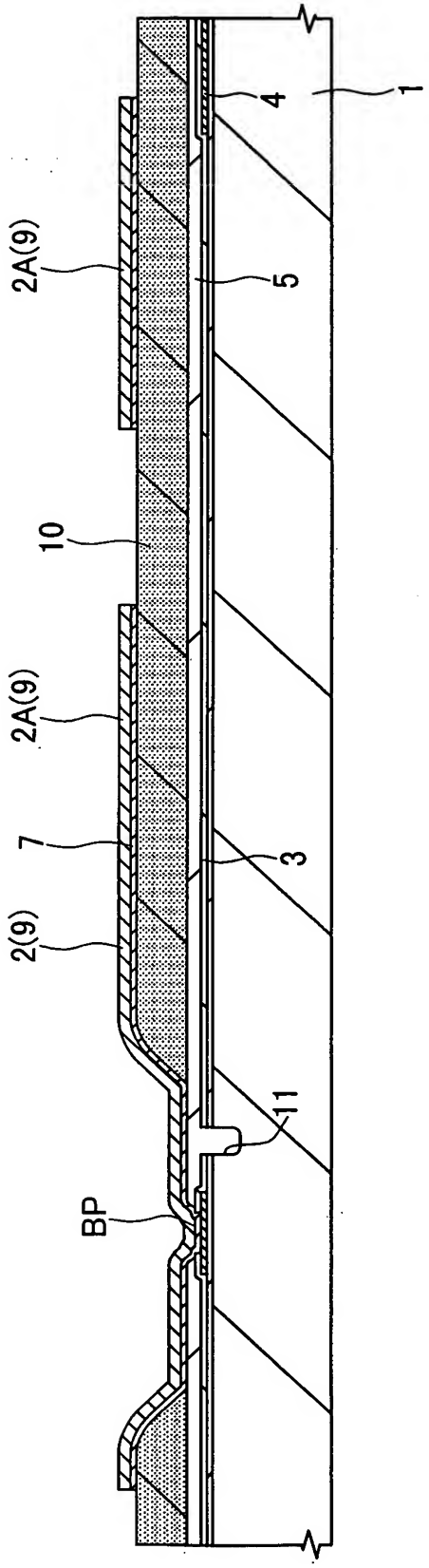


FIG.24

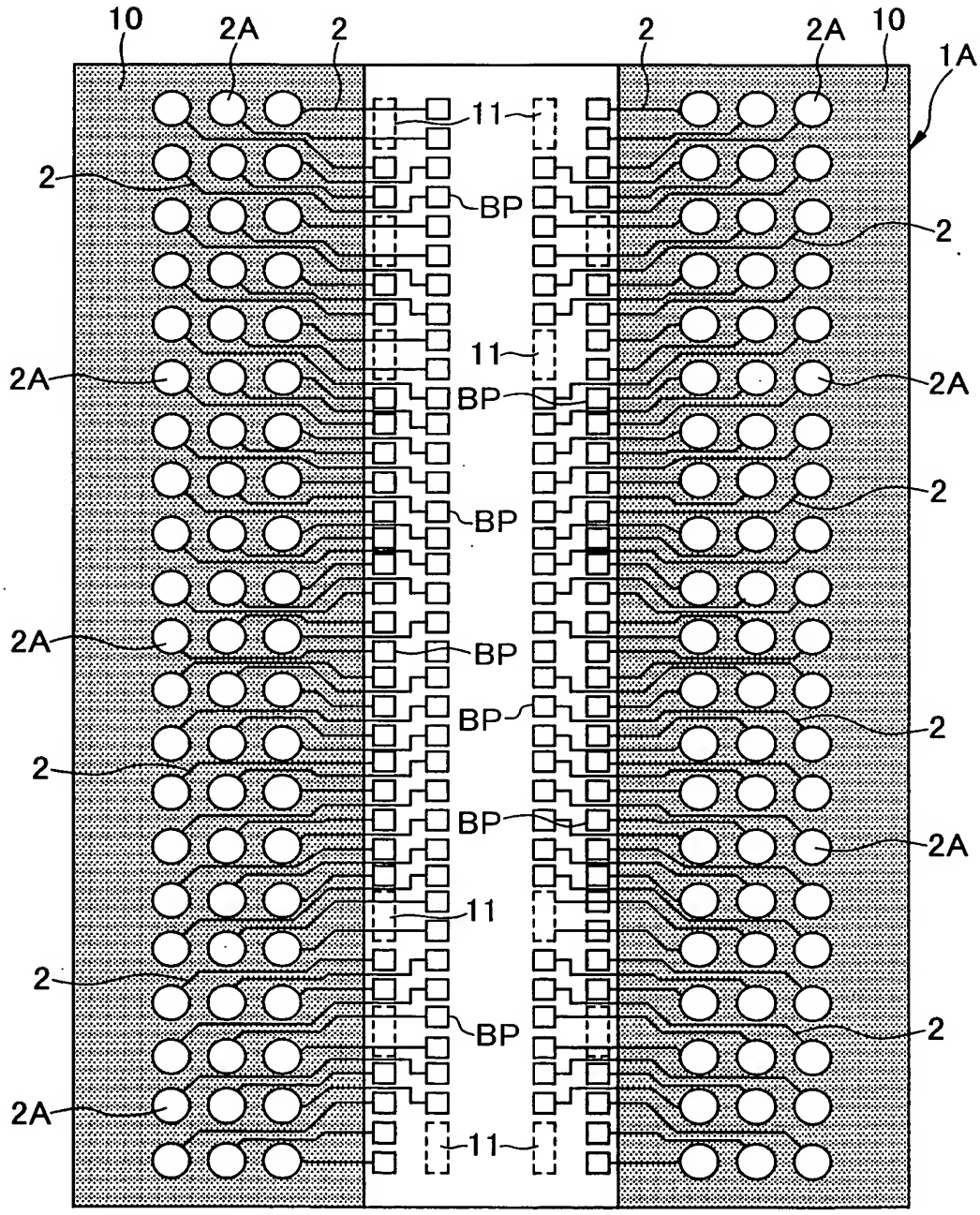

10
2A
2
2
2A
10
1A
11
2
BP
2
11
2A
BP
2A
2
BP
BP
2A
2
BP
2
BP
2A
11
2
BP
2
2A
11

FIG.25

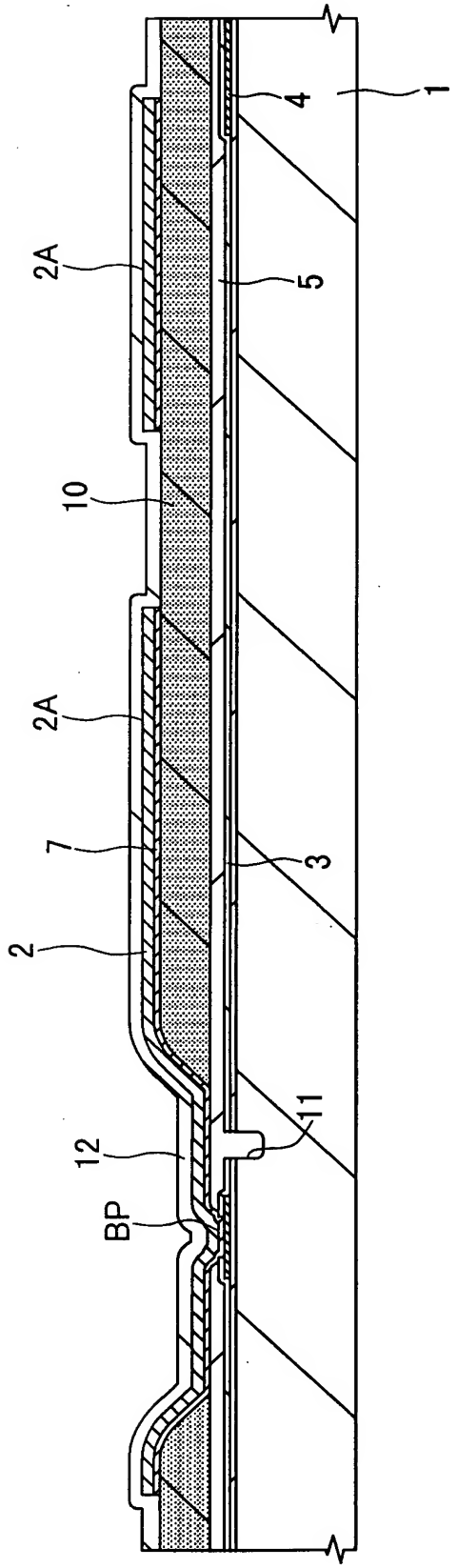


FIG.26

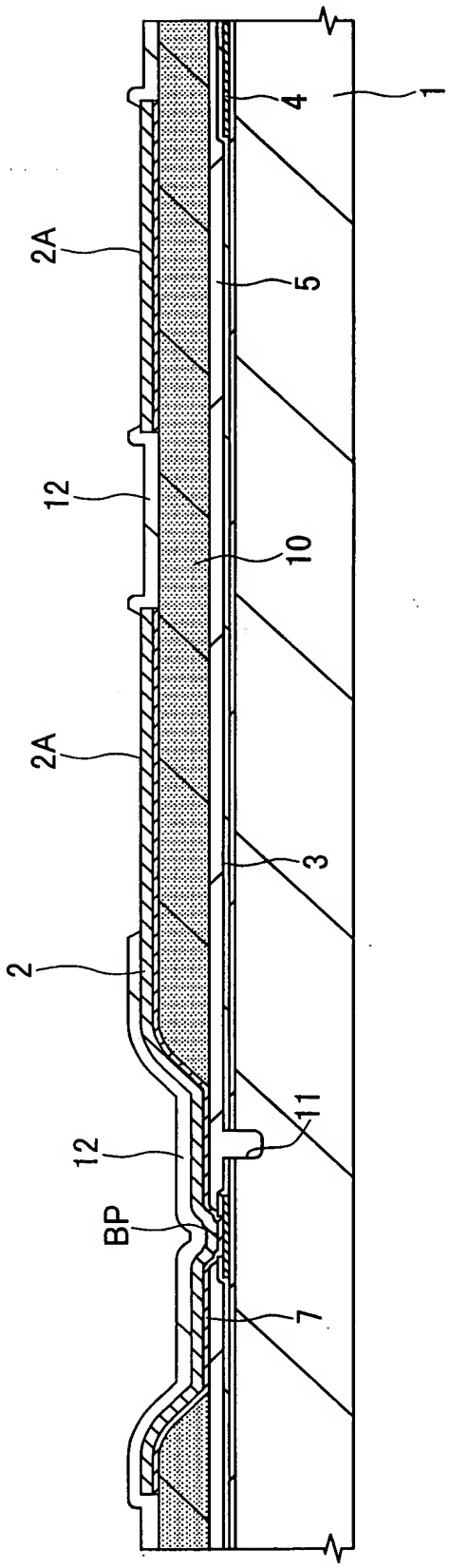


FIG.27

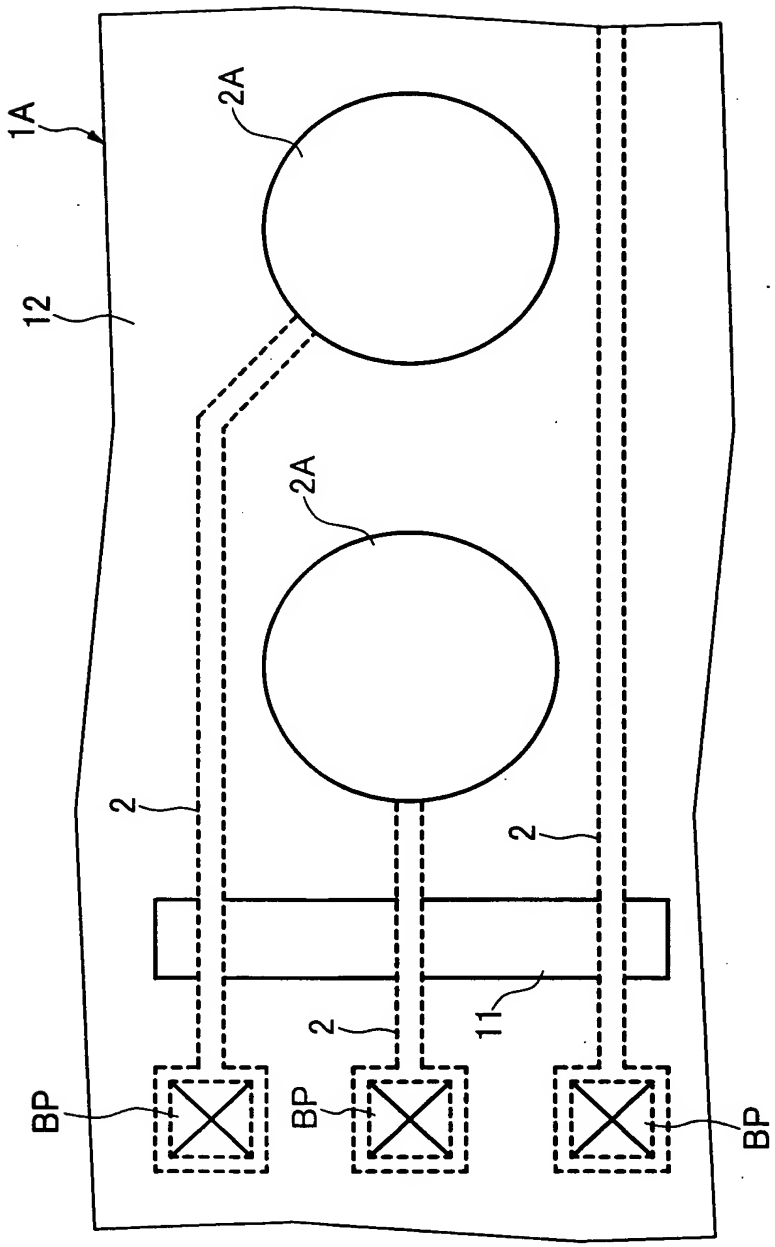


FIG.28

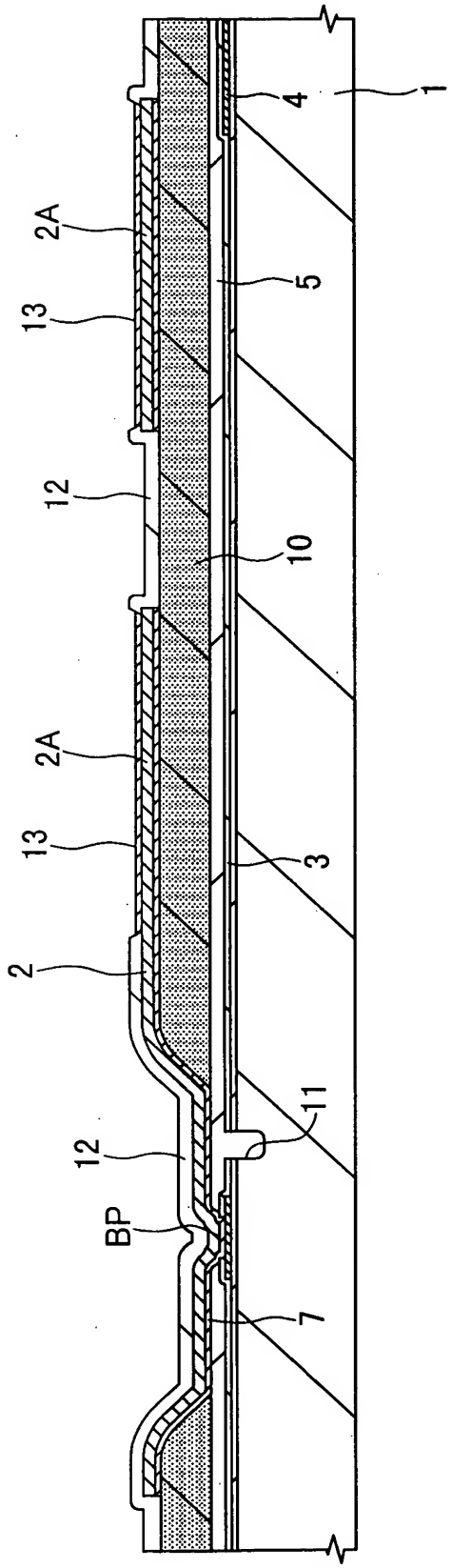


FIG.29

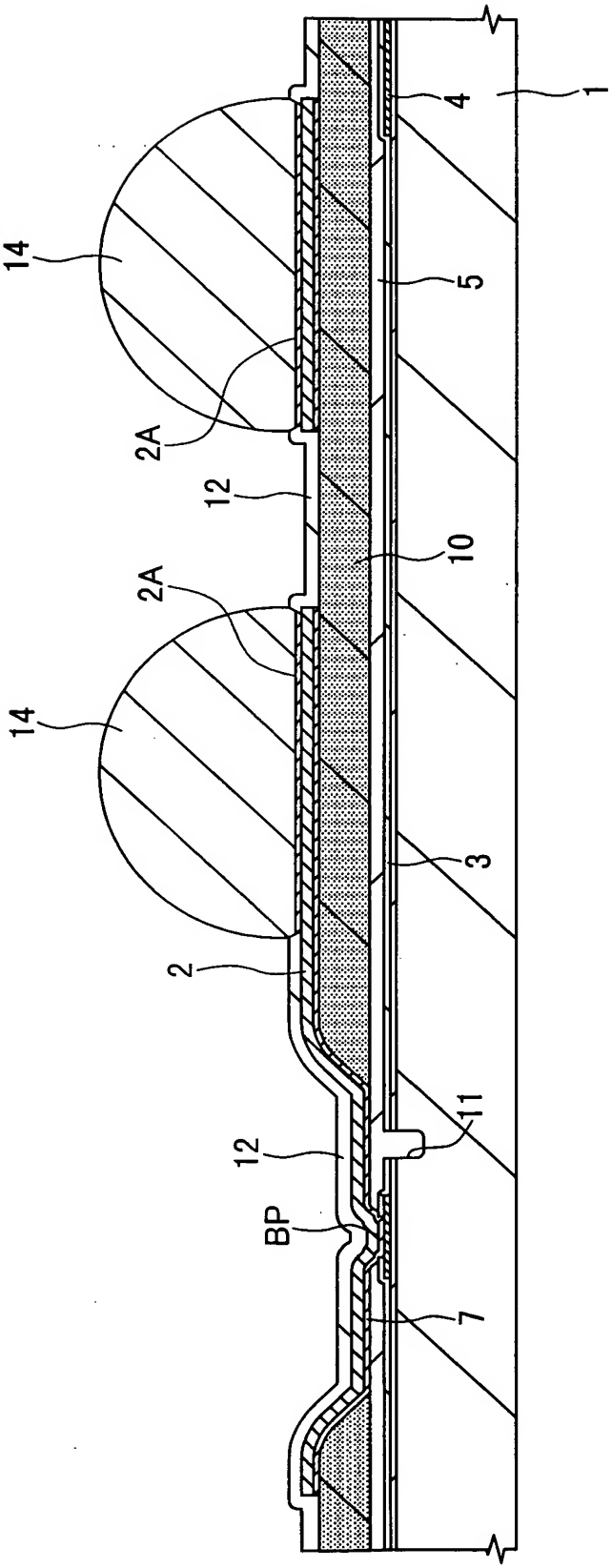


FIG.30

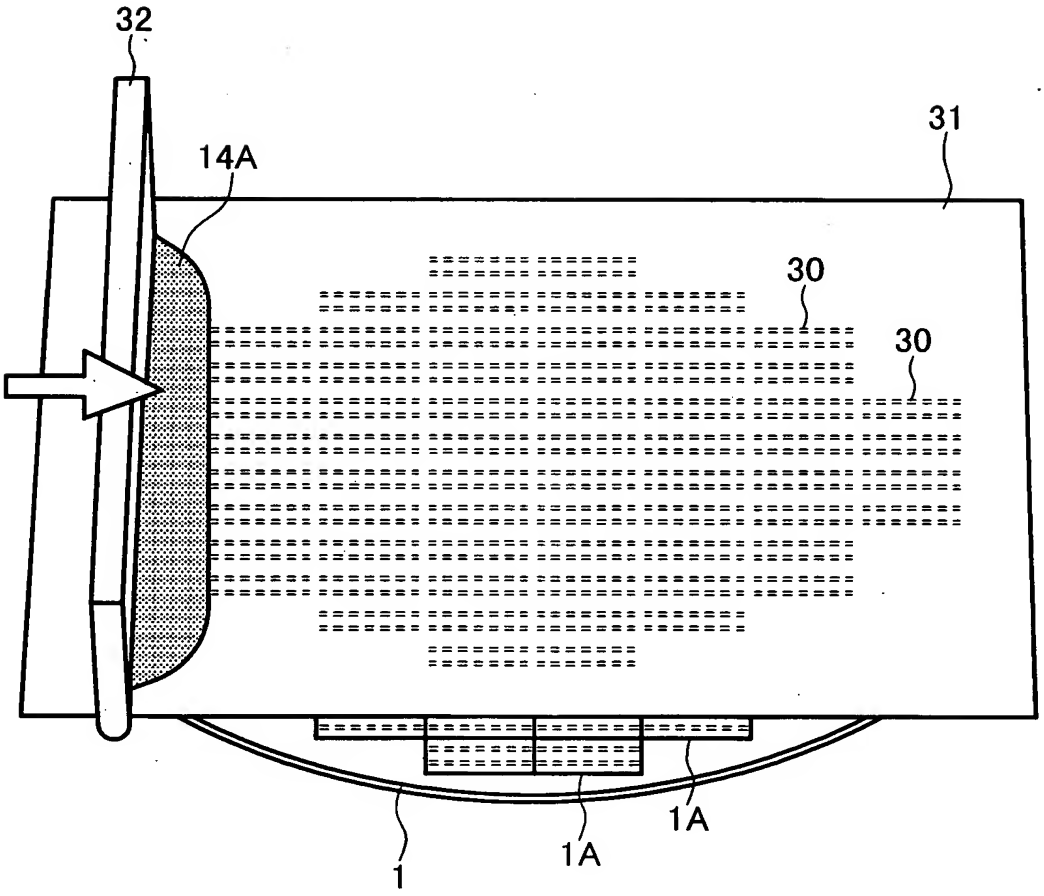


FIG.31

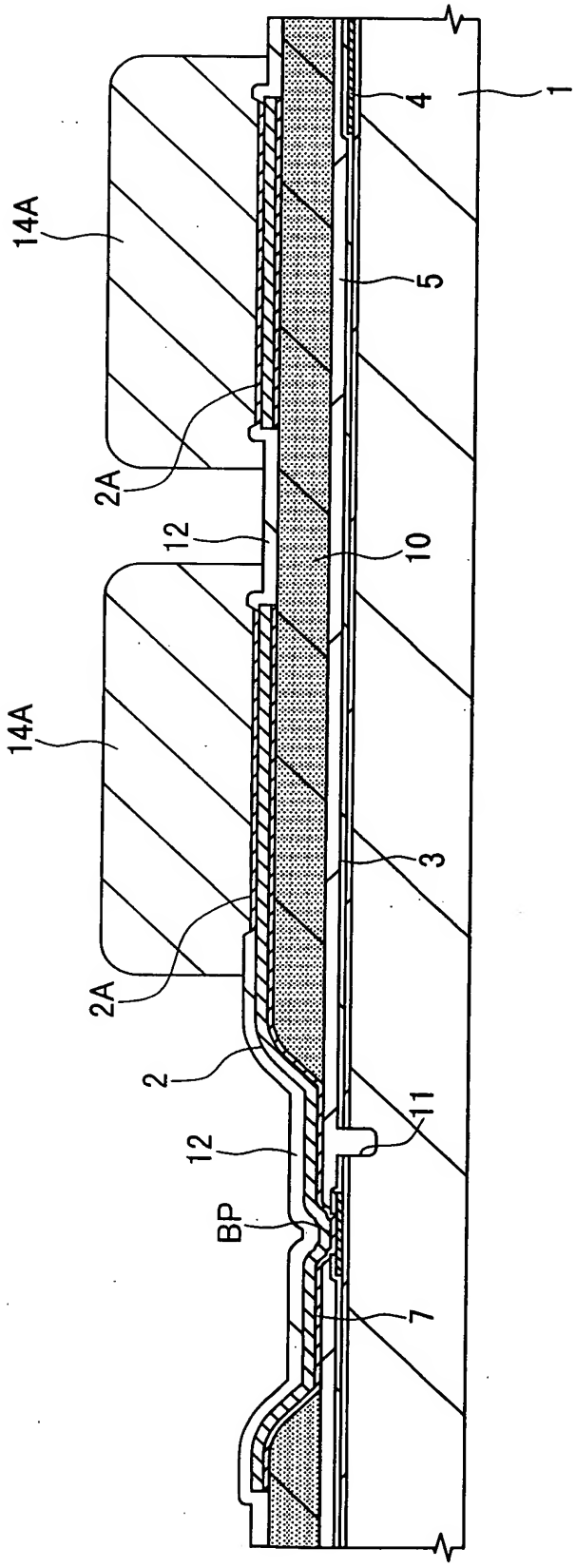


FIG.32

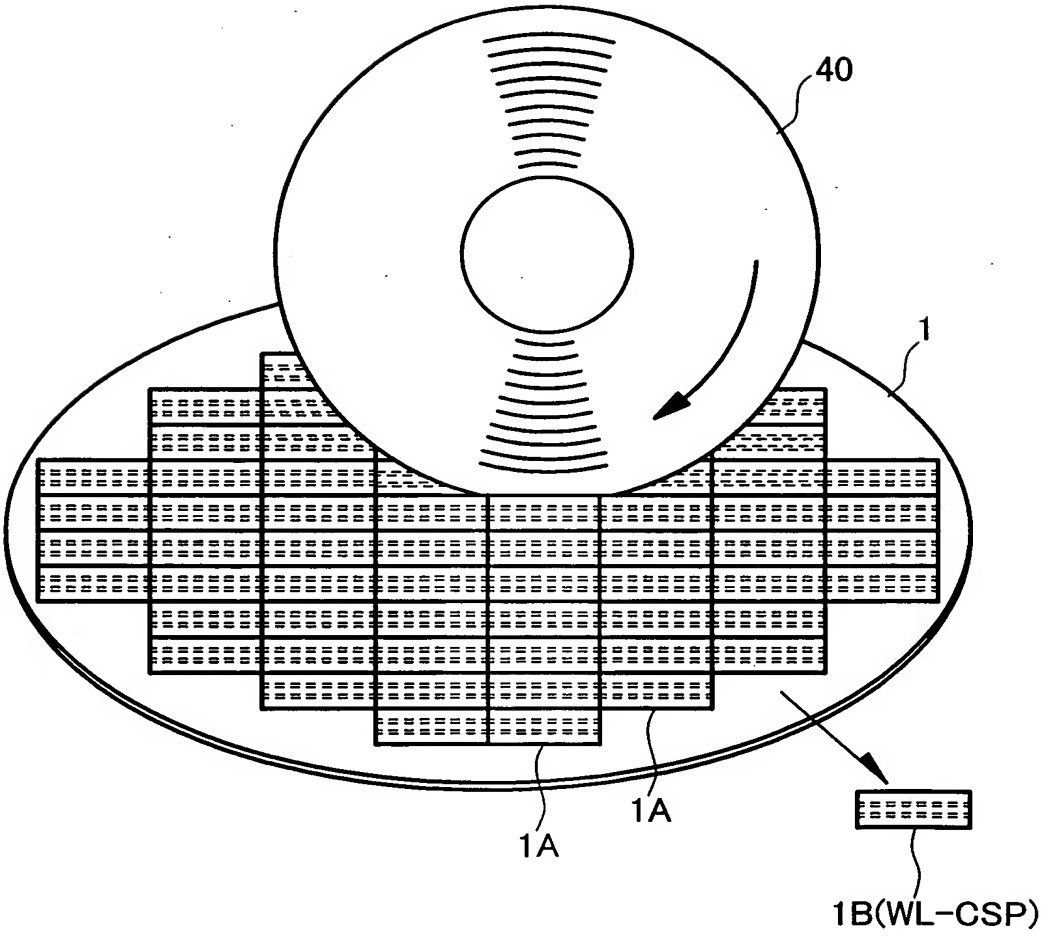


FIG.33

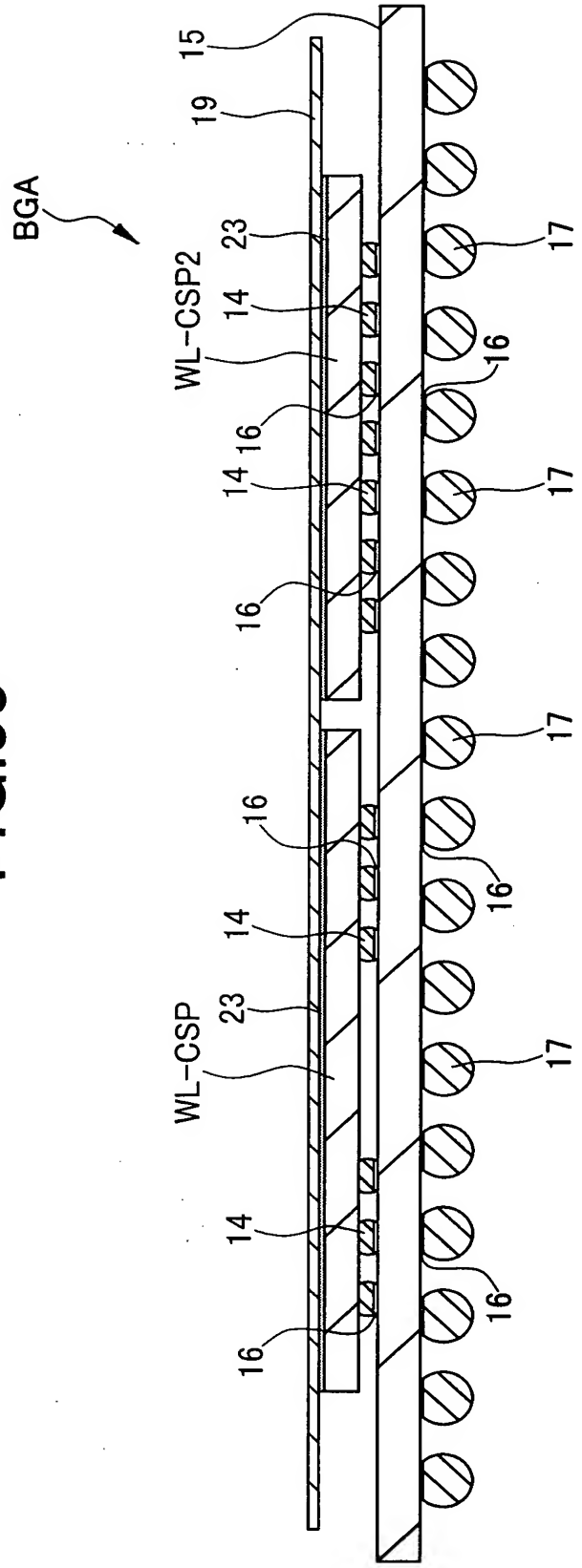


FIG.34

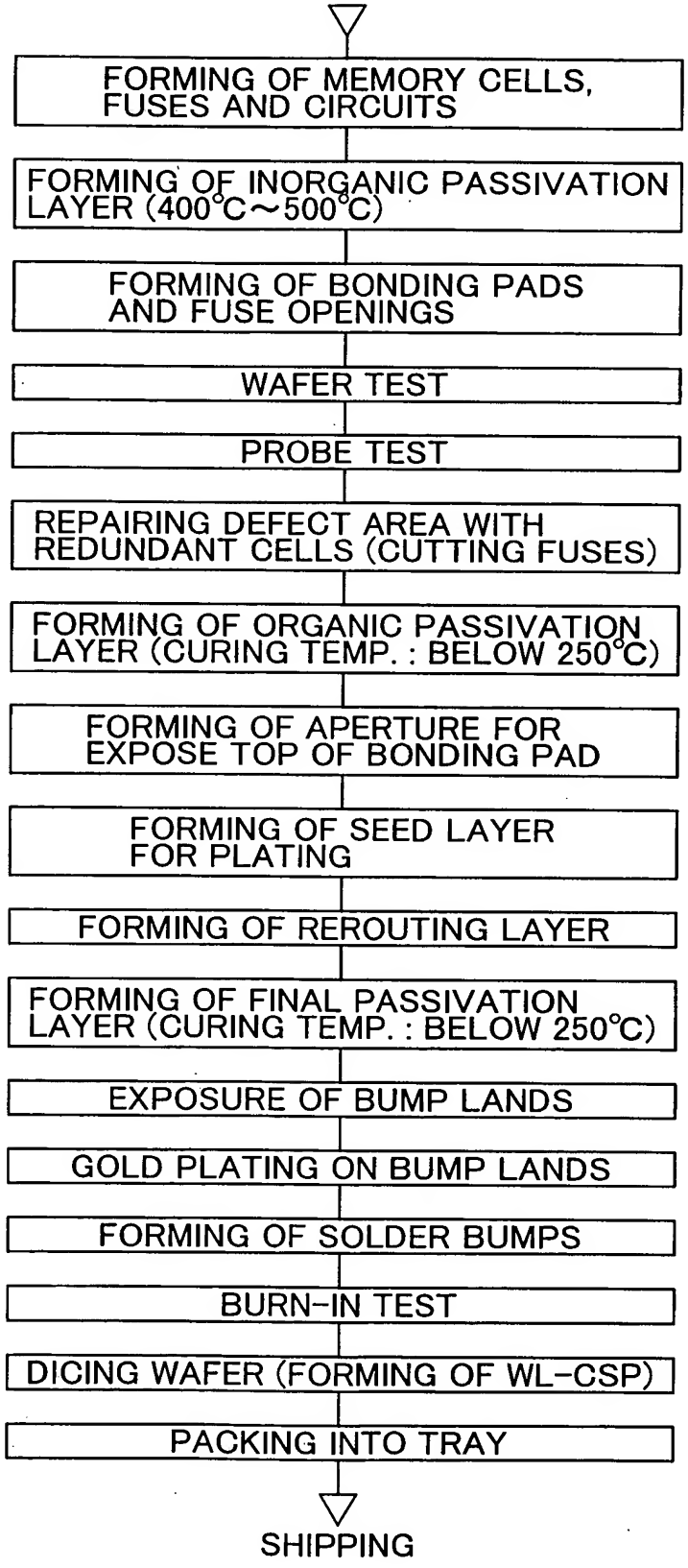
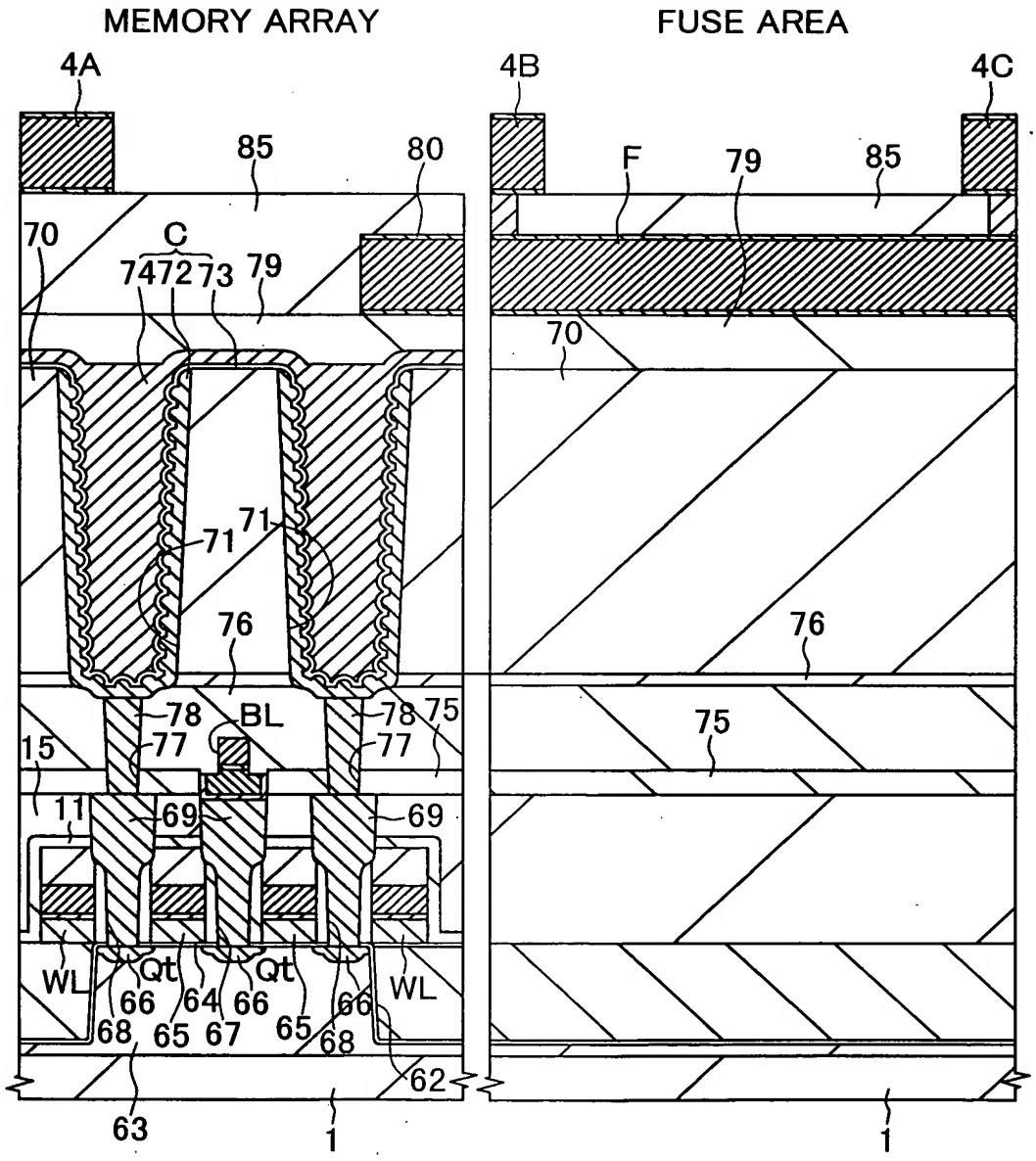

FORMING OF MEMORY CELLS, FUSES AND CIRCUITS
FORMING OF INORGANIC PASSIVATION LAYER (400°C~500°C)
FORMING OF BONDING PADS AND FUSE OPENINGS
WAFER TEST
PROBE TEST
REPAIRING DEFECT AREA WITH REDUNDANT CELLS (CUTTING FUSES)
FORMING OF ORGANIC PASSIVATION LAYER (CURING TEMP. : BELOW 250°C)
FORMING OF APERTURE FOR EXPOSE TOP OF BONDING PAD
FORMING OF SEED LAYER FOR PLATING
FORMING OF REROUTING LAYER
FORMING OF FINAL PASSIVATION LAYER (CURING TEMP. : BELOW 250°C)
EXPOSURE OF BUMP LANDS
GOLD PLATING ON BUMP LANDS
FORMING OF SOLDER BUMPS
BURN-IN TEST
DICING WAFER (FORMING OF WL-CSP)
PACKING INTO TRAY
SHIPPING

FIG.35


MEMORY ARRAY
FUSE AREA
4A
4B
4C
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80
F
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73
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71
76
76
78
BL
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77
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69
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WL
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Qt
WL
66
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66
66
68
65
67
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68
62
63
1
1

FIG.36

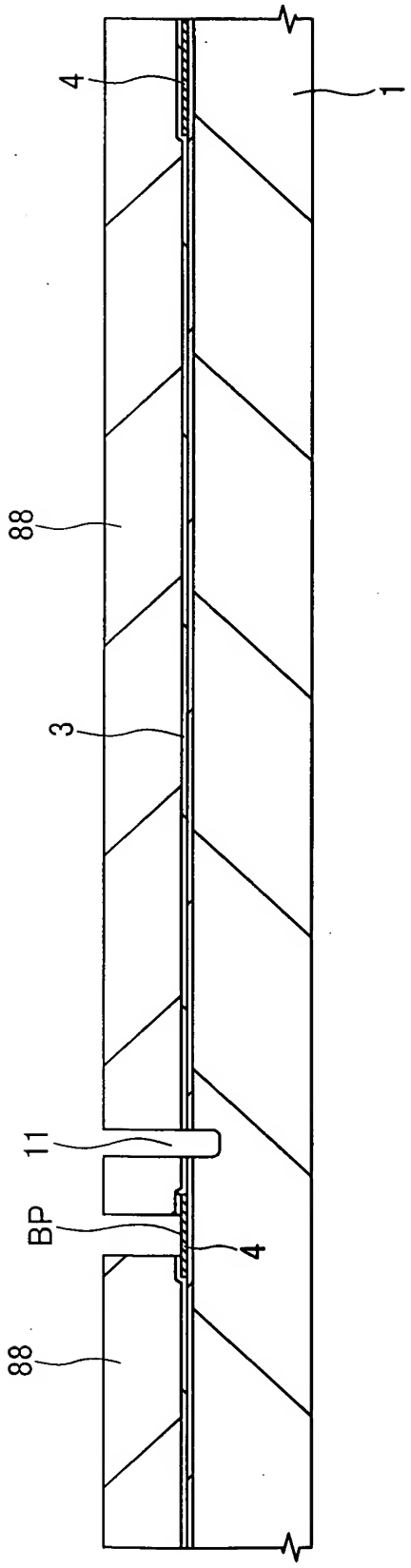
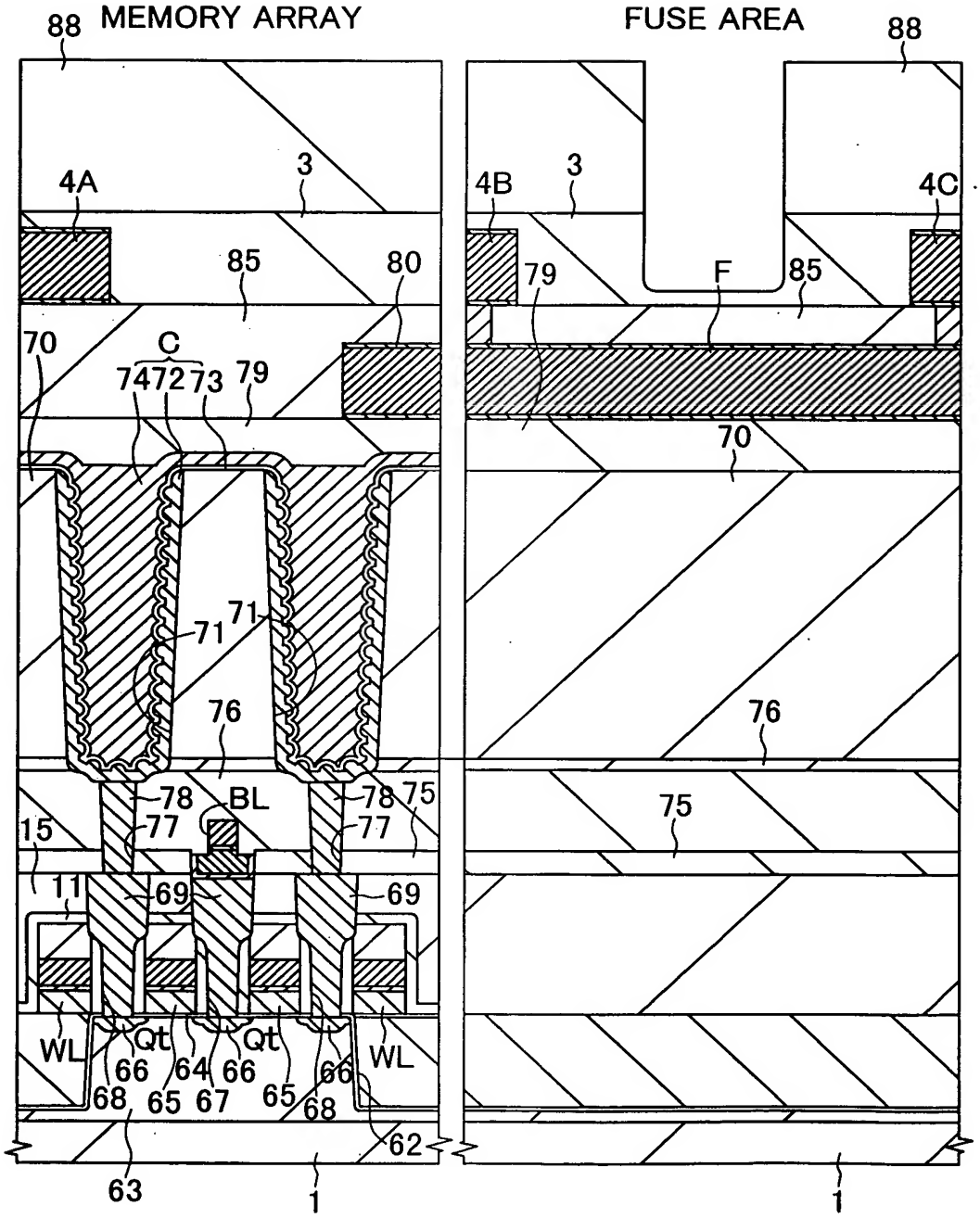


FIG.37


88
MEMORY ARRAY
FUSE AREA
88
4A
3
4B
3
4C
85
80
79
F
85
70
C
74
72
73
79
70
71
71
76
76
78
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78
75
77
77
75
15
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67
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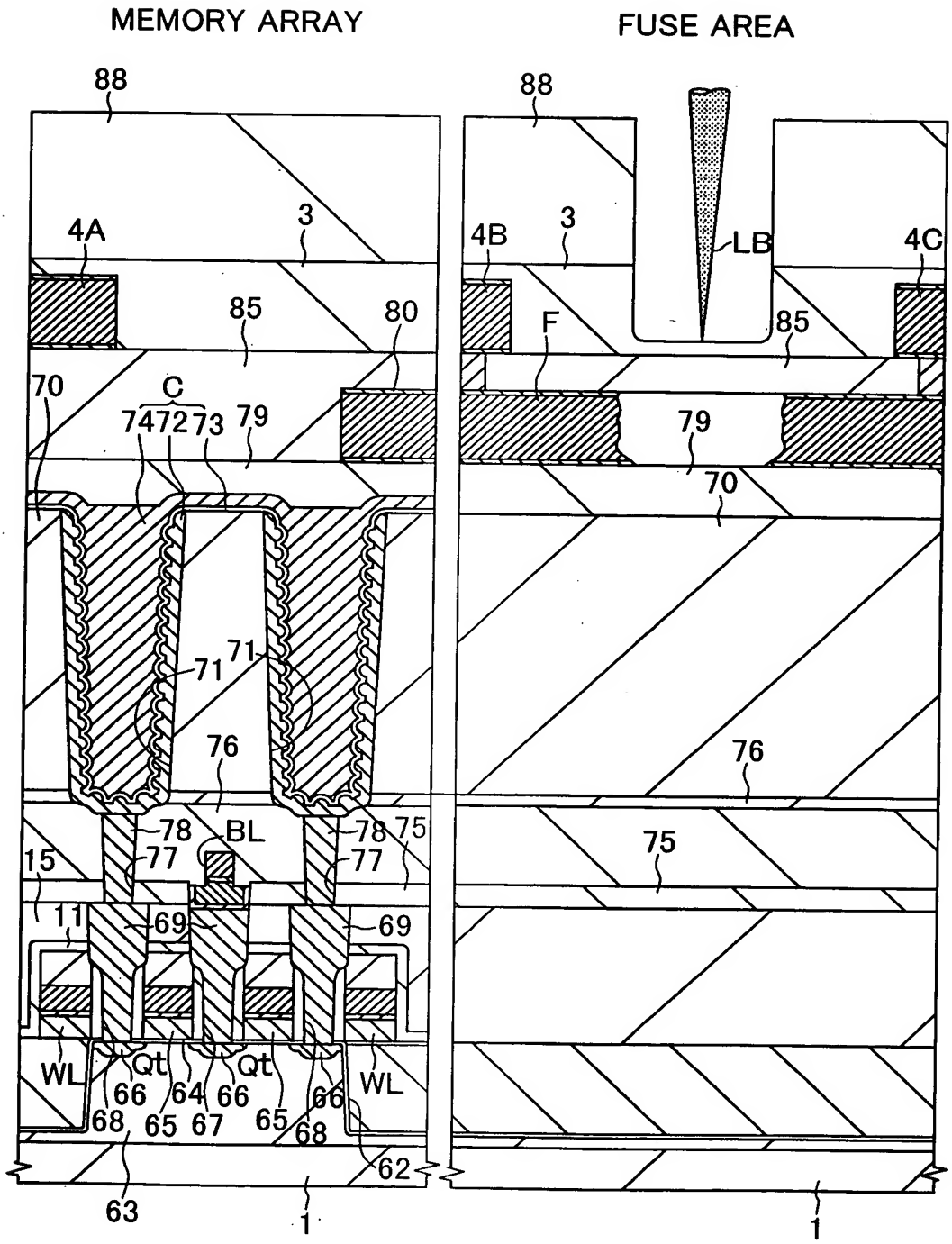
68
62
63
1
1

FIG.38


MEMORY ARRAY
FUSE AREA
88
88
4A
3
4B
3
LB
4C
85
80
F
85
70
C
74 72 73
79
79
70
71
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67
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68
62
63
1
1

FIG.39

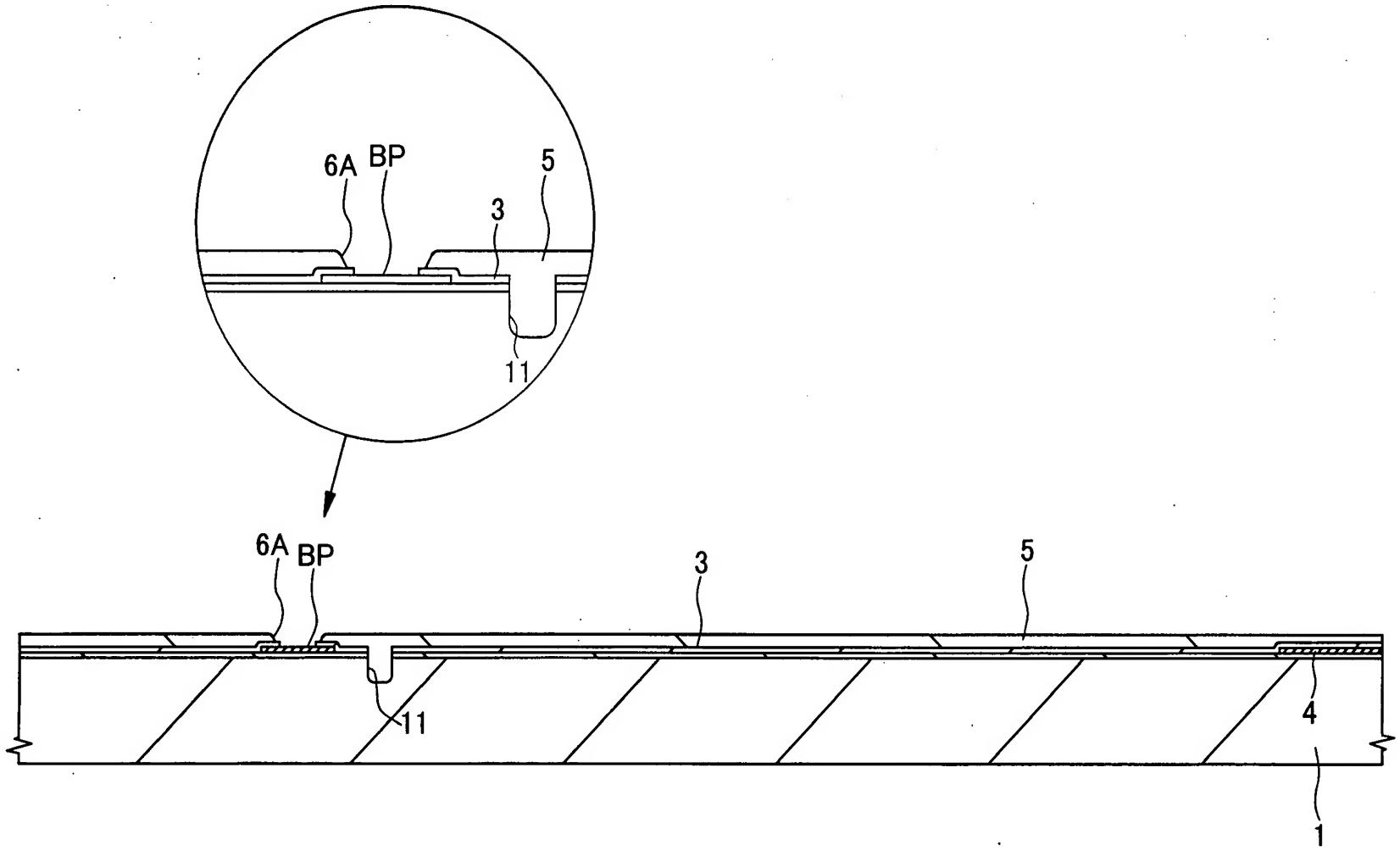

FIG.40

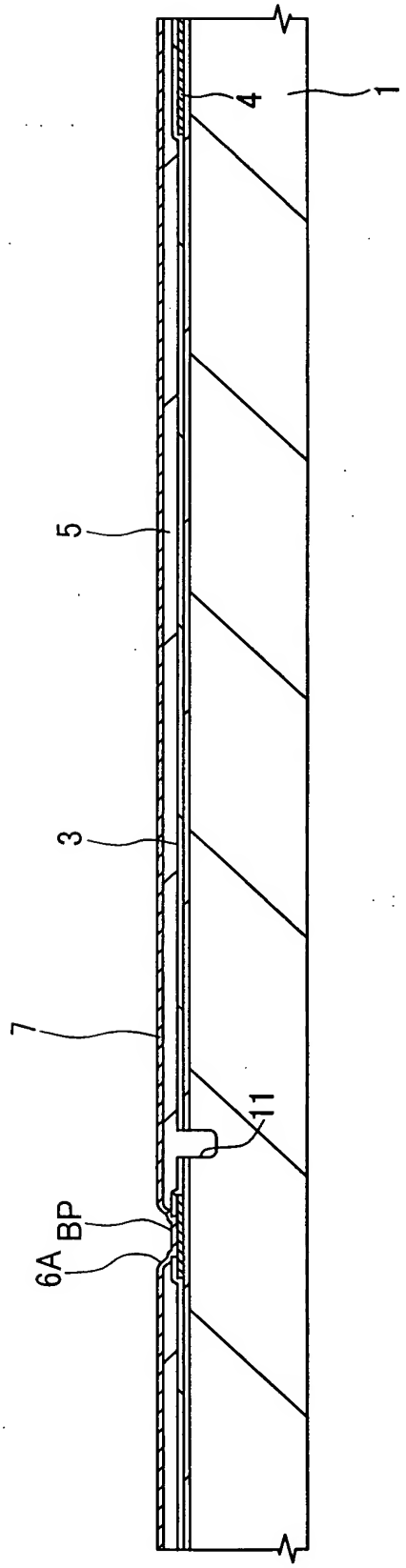

FIG.41

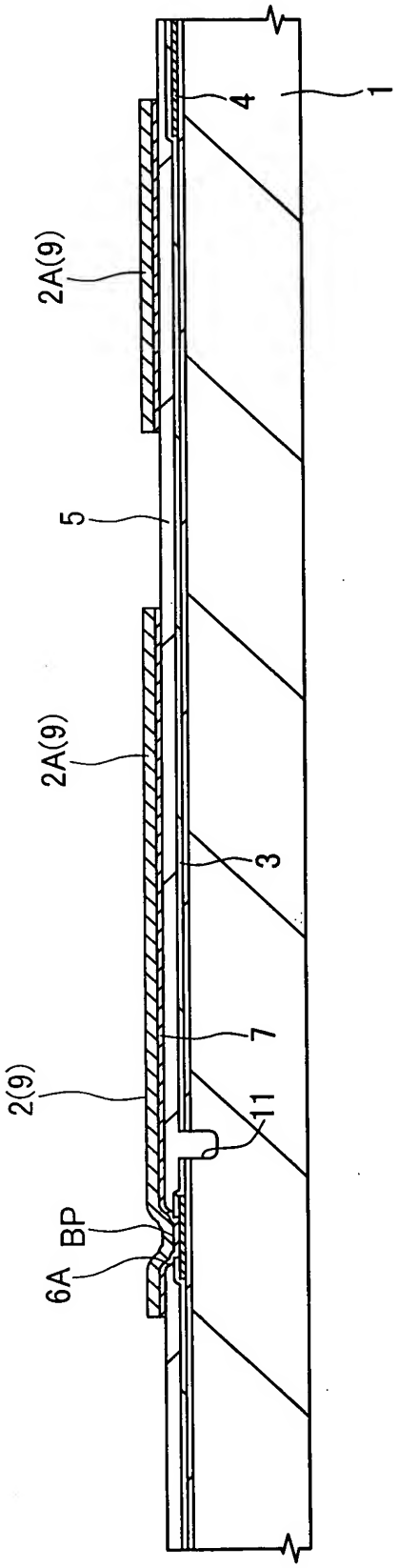

FIG.42

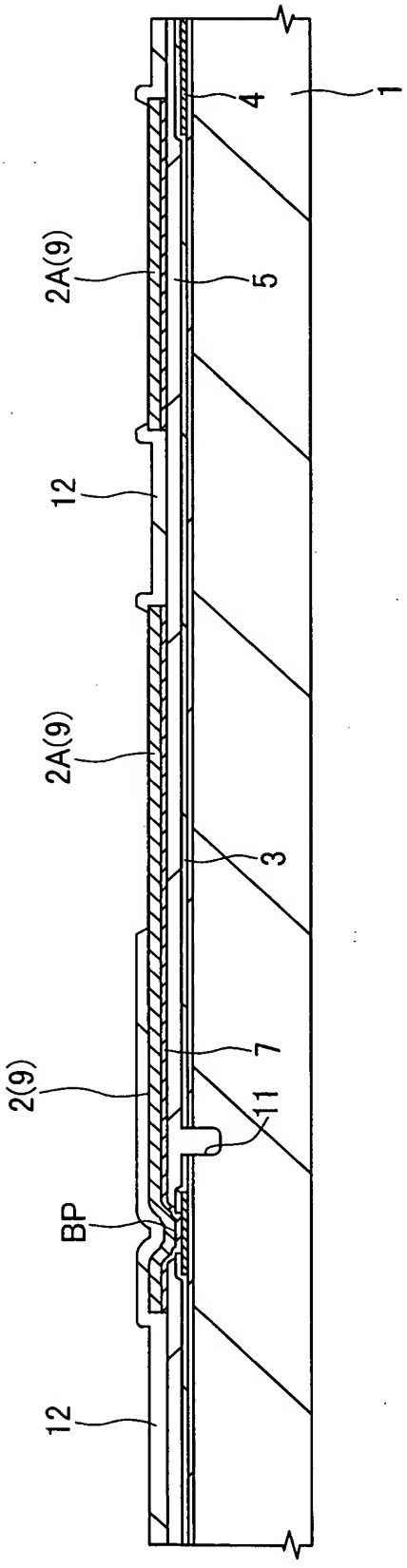

FIG.43

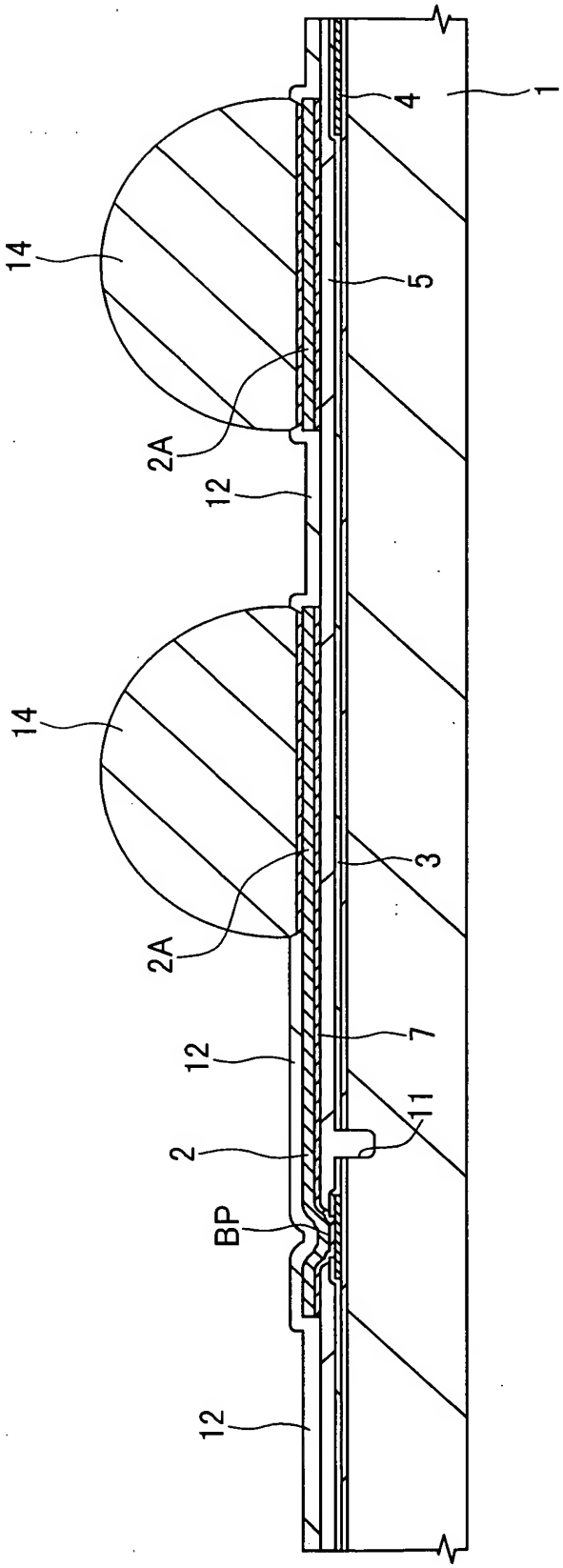

FIG.44

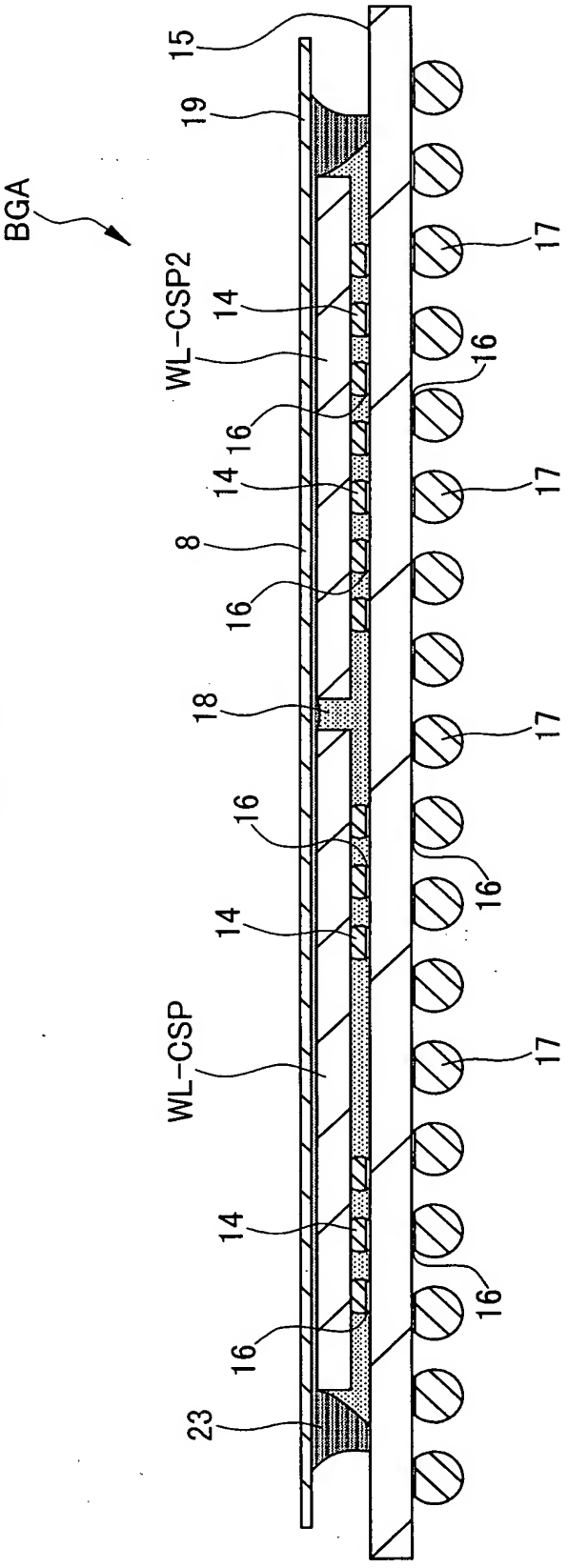

FIG.45

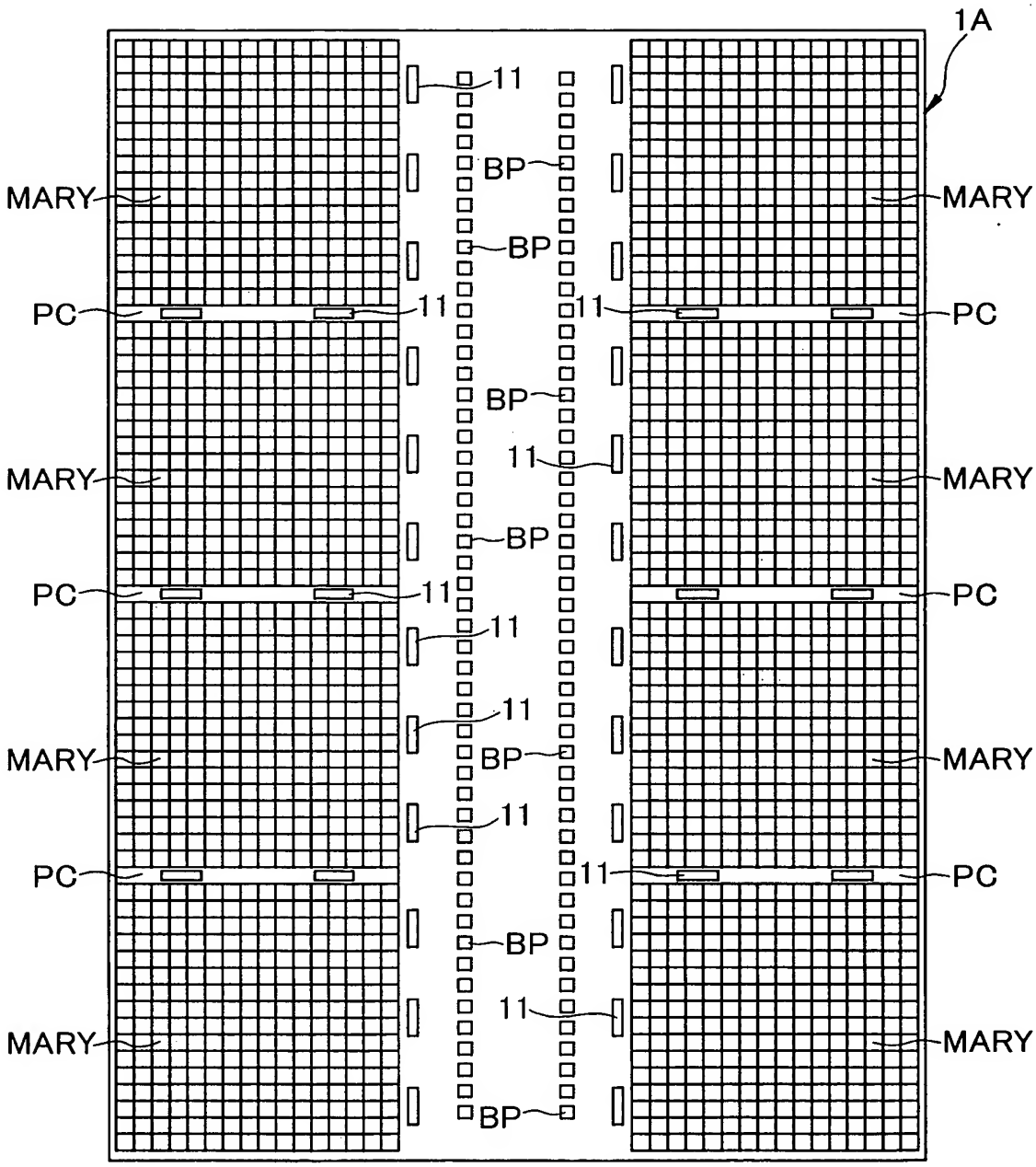

FIG.46

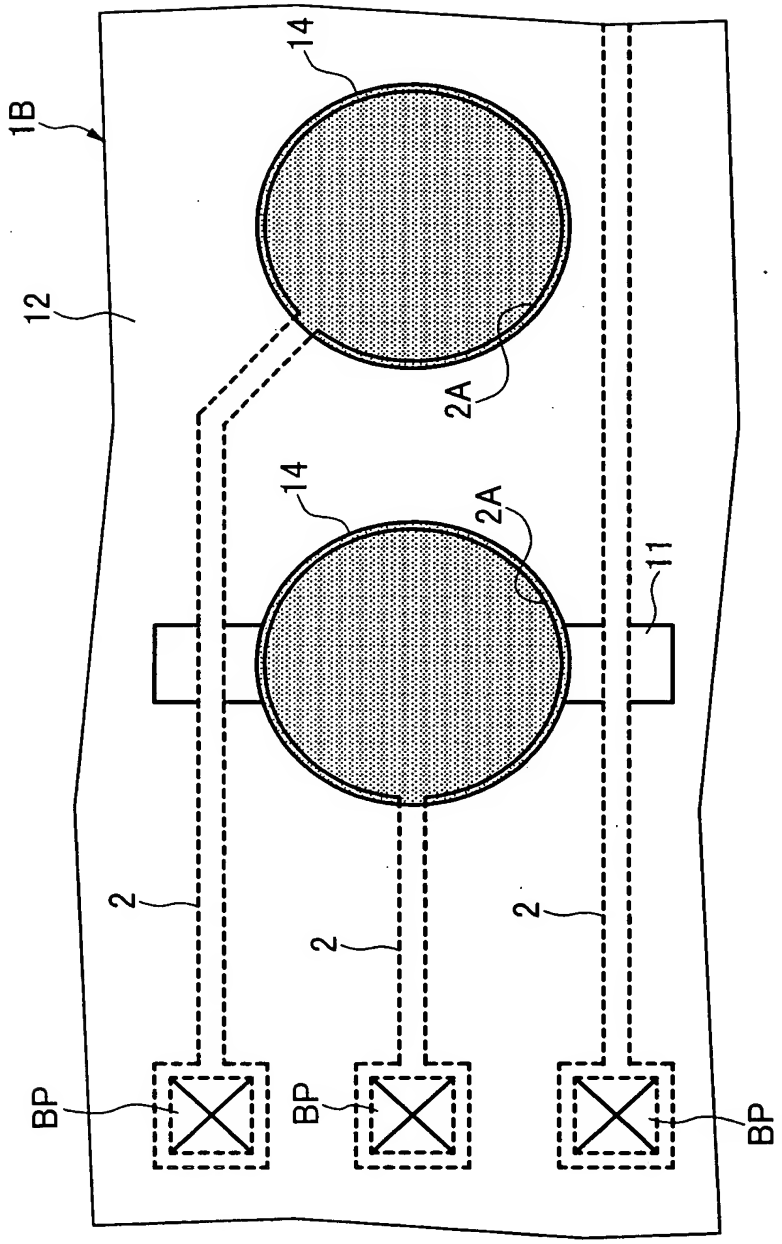

FIG.47

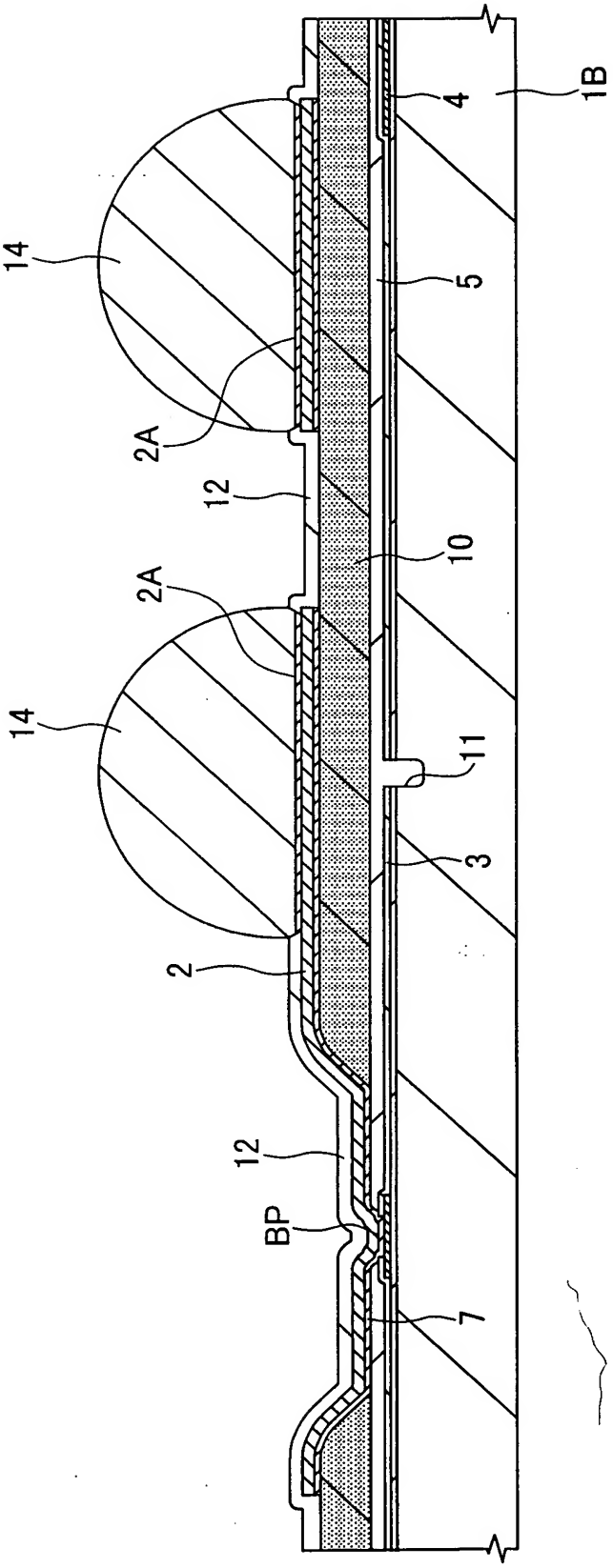

FIG.48

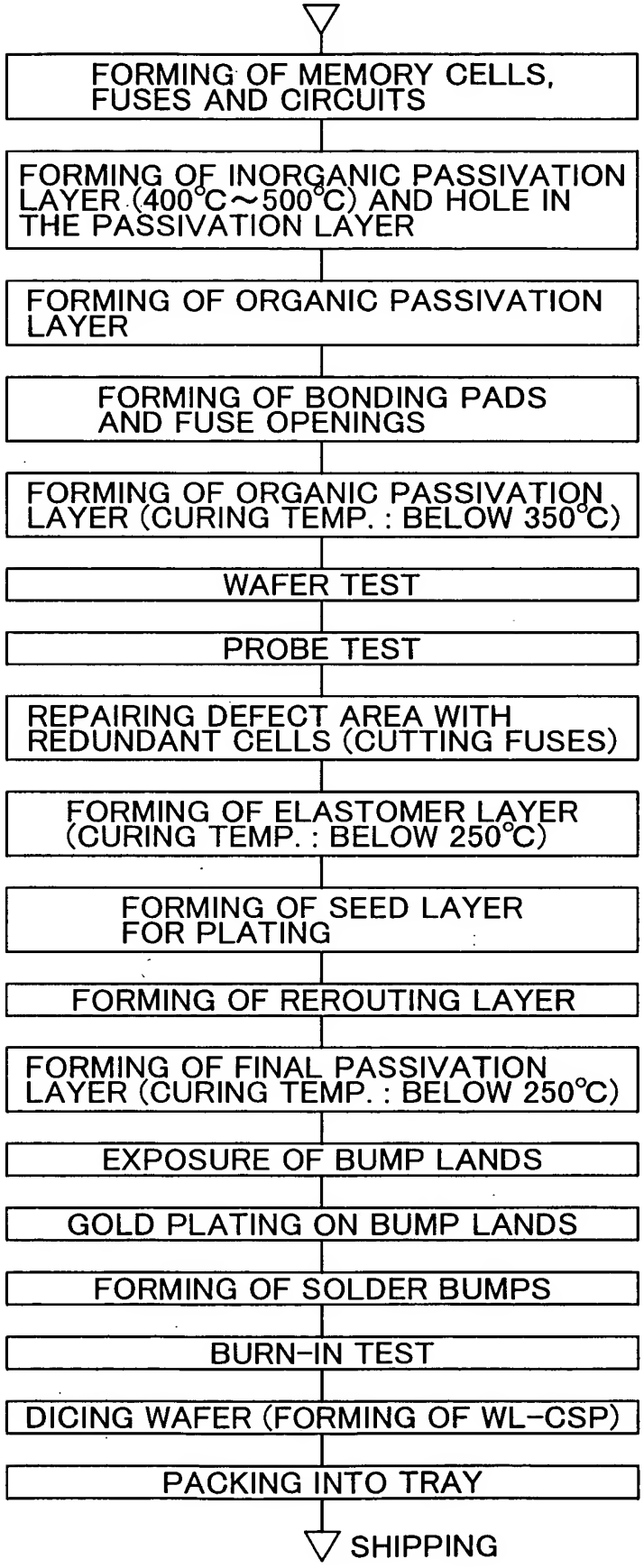
FORMING OF MEMORY CELLS, FUSES AND CIRCUITS
FORMING OF INORGANIC PASSIVATION LAYER (400°C～500°C) AND HOLE IN THE PASSIVATION LAYER
FORMING OF ORGANIC PASSIVATION LAYER
FORMING OF BONDING PADS AND FUSE OPENINGS
FORMING OF ORGANIC PASSIVATION LAYER (CURING TEMP. : BELOW 350°C)
WAFER TEST
PROBE TEST
REPAIRING DEFECT AREA WITH REDUNDANT CELLS (CUTTING FUSES)
FORMING OF ELASTOMER LAYER (CURING TEMP. : BELOW 250°C)
FORMING OF SEED LAYER FOR PLATING
FORMING OF REROUTING LAYER
FORMING OF FINAL PASSIVATION LAYER (CURING TEMP. : BELOW 250°C)
EXPOSURE OF BUMP LANDS
GOLD PLATING ON BUMP LANDS
FORMING OF SOLDER BUMPS
BURN-IN TEST
DICING WAFER (FORMING OF WL-CSP)
PACKING INTO TRAY
SHIPPING

FIG.49

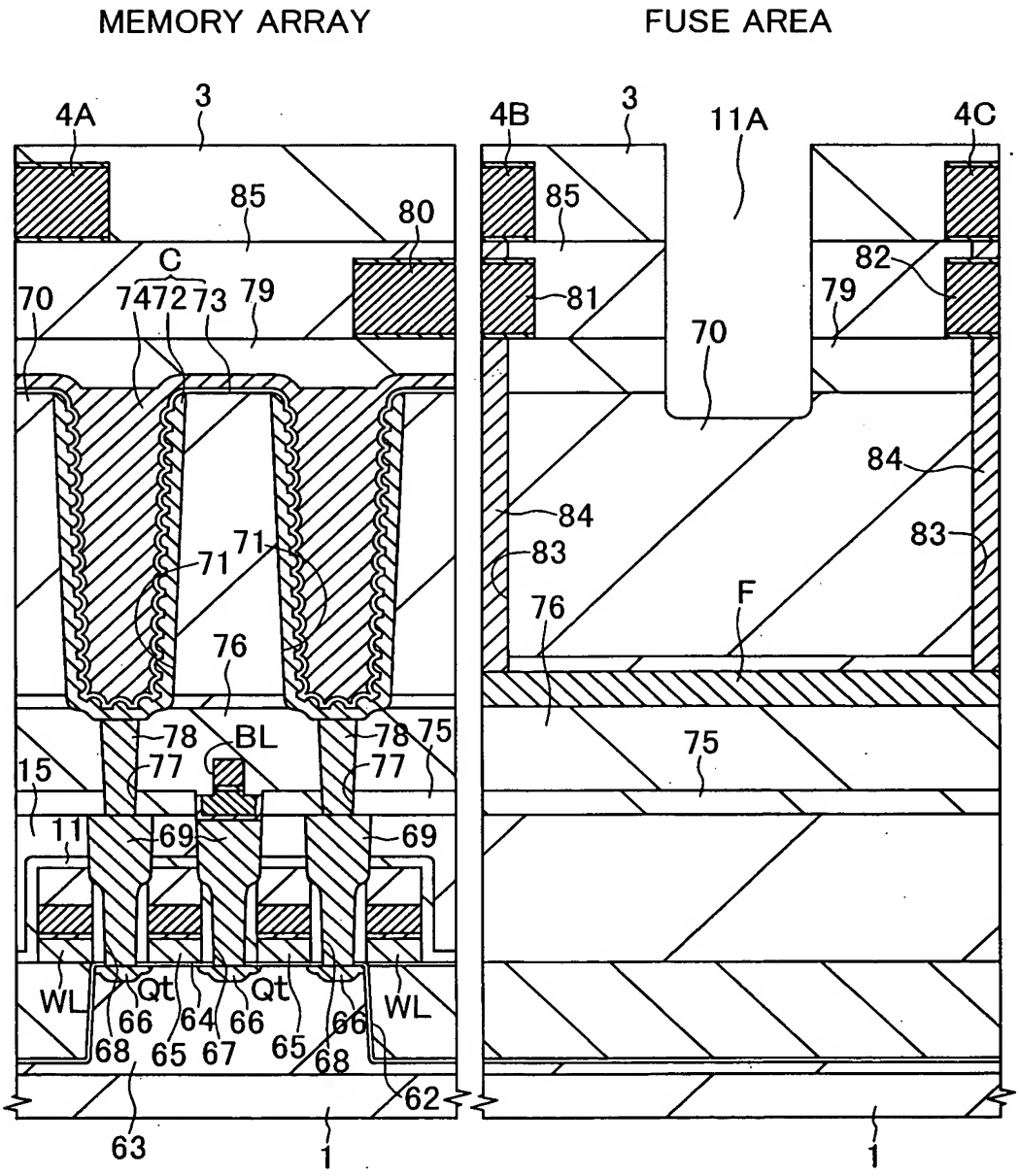
MEMORY ARRAY
FUSE AREA
4A
3
4B
3
11A
4C
85
80
85
82
C
70
74
72
73
79
81
79
70
84
84
71
71
83
83
F
76
76
78
BL
78
75
77
77
75
15
11
69
69
WL
Qt
Qt
WL
66
64
66
66
68
65
67
65
68
62
63
1
1

FIG.50

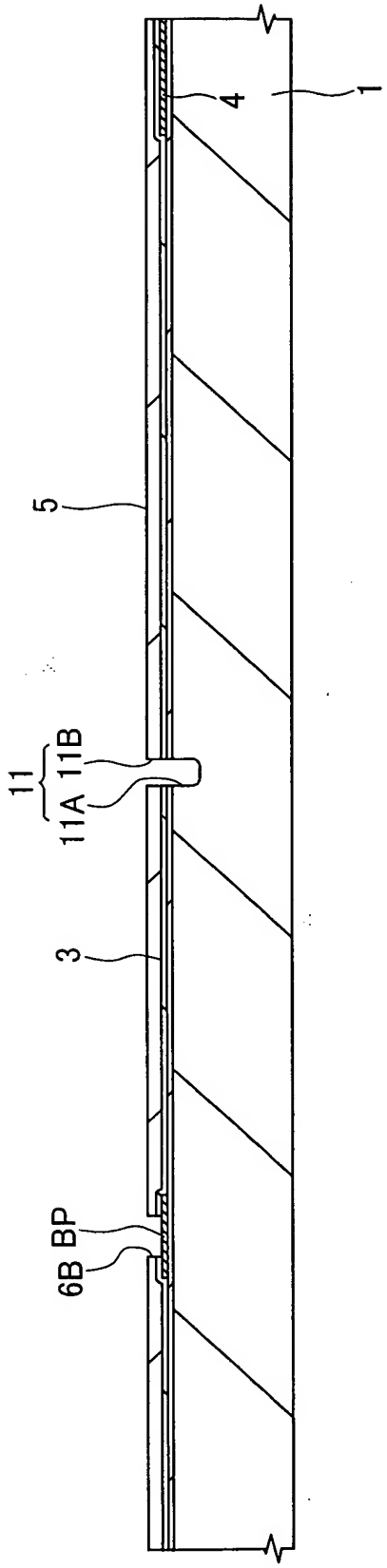

FIG.51

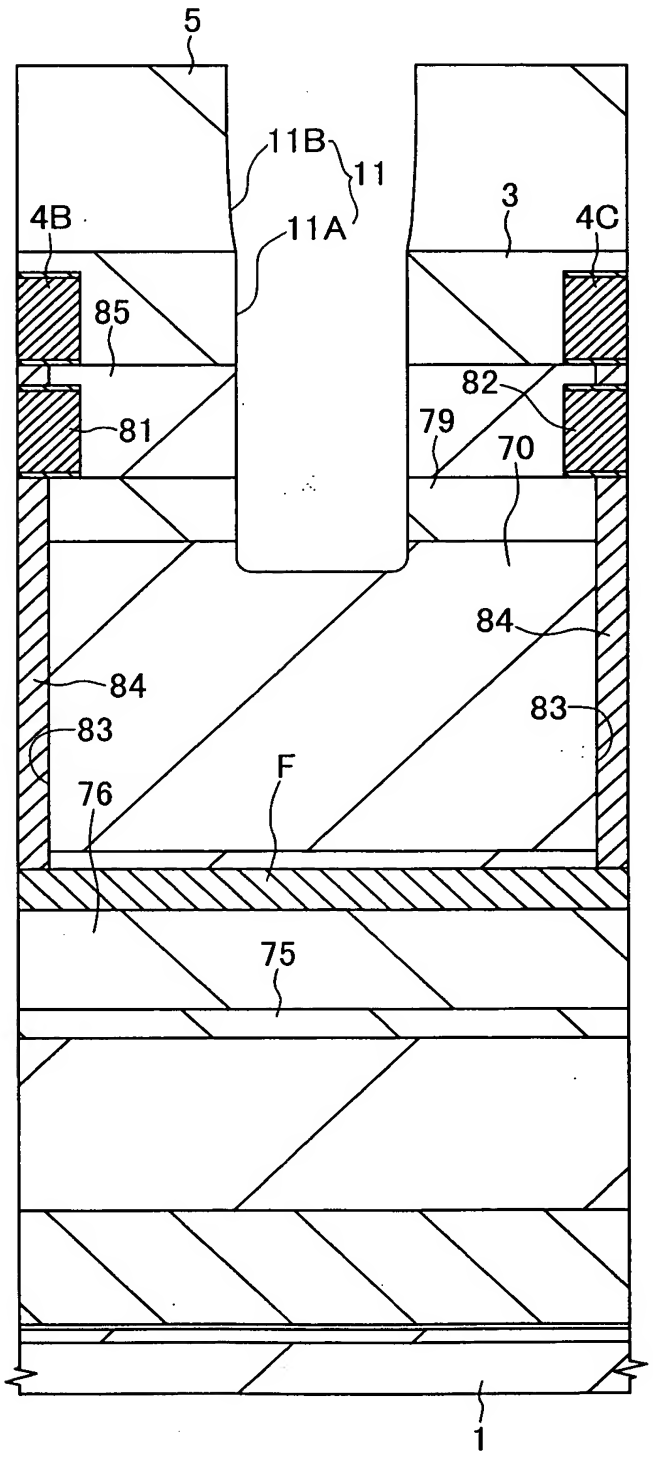

FIG.52

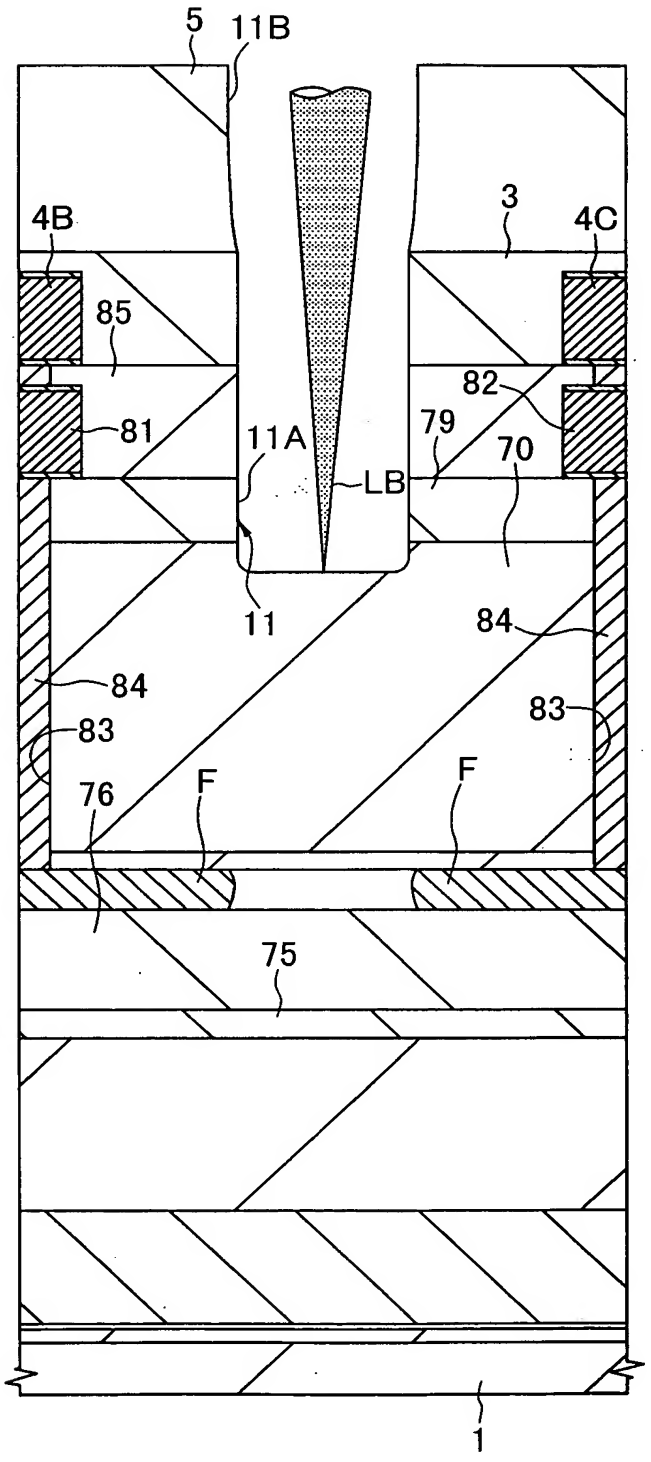

FIG.53

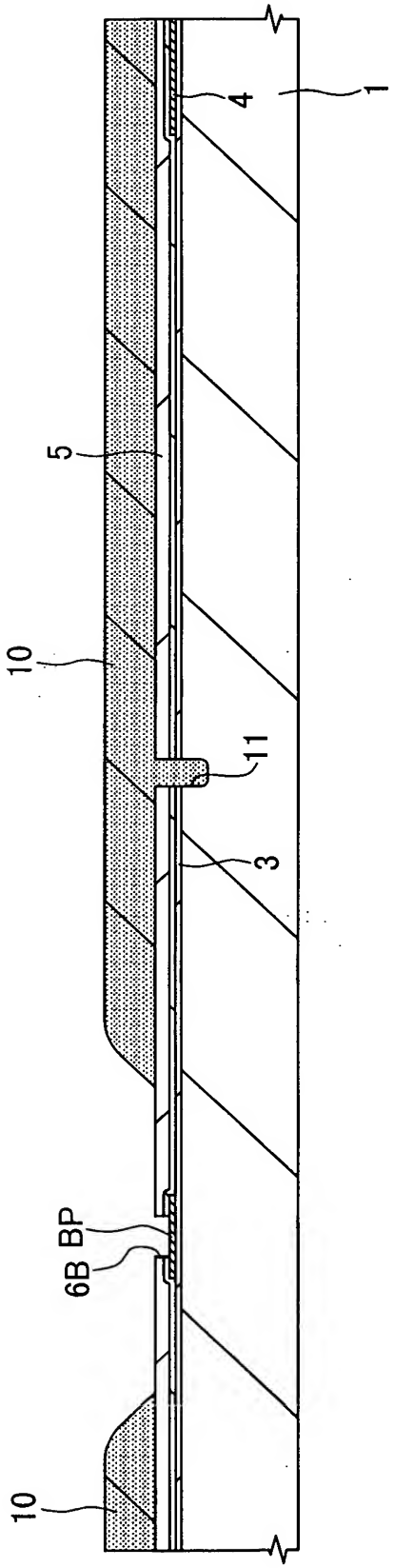

FIG.54

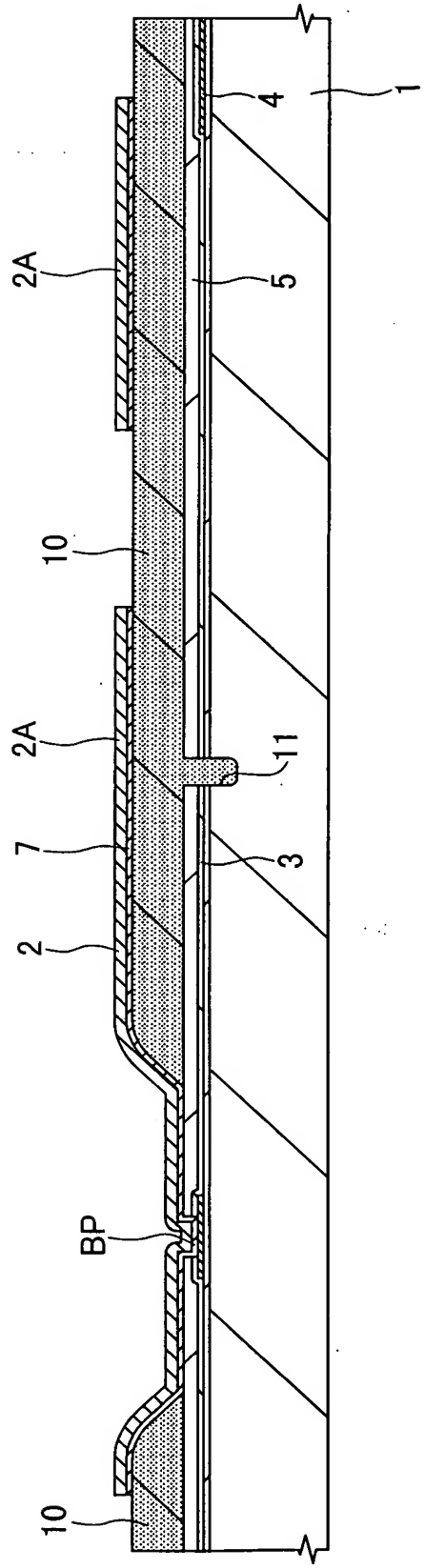

FIG.55

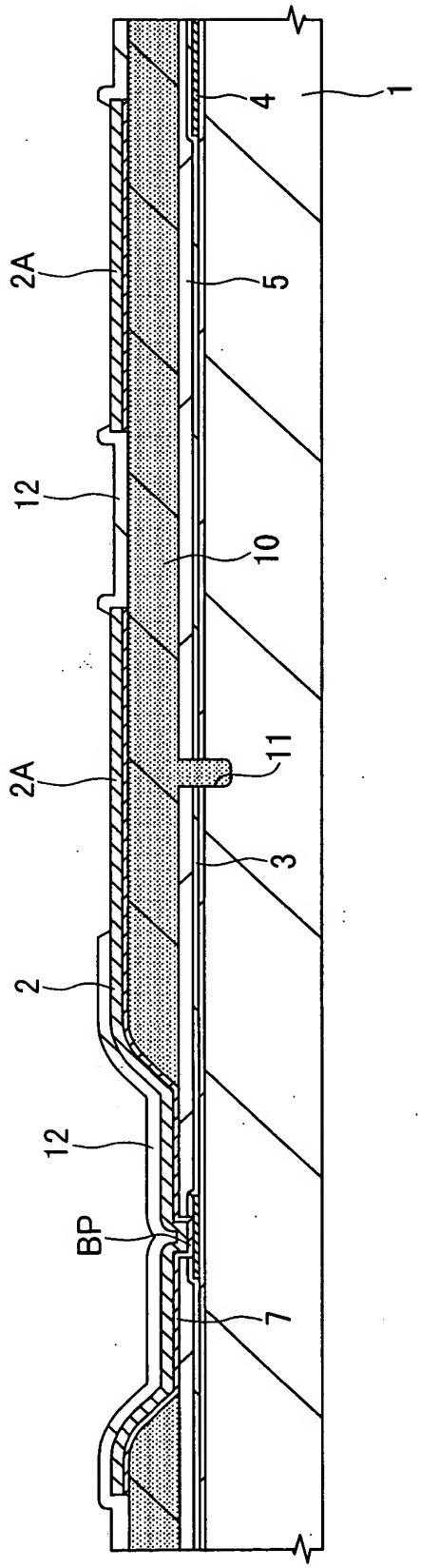

FIG.56